# A Double Grounded Transformerless Photovoltaic Array String Inverter with Film Capacitors and Silicon Carbide Transistors

by

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ABSTRACT

A new photovoltaic (PV) array power converter circuit is presented. The salient features of this inverter are: transformerless topology, grounded PV array, and only film capacitors. The motivations are to reduce cost, eliminate leakage ground currents, and improve reliability. The use of Silicon Carbide (SiC) transistors is the key enabling technology for this particular circuit to attain good efficiency.

Traditionally, grid connected PV inverters required a transformer for isolation and safety. The disadvantage of high frequency transformer based inverters is complexity and cost. Transformerless inverters have become more popular recently, although they can be challenging to implement because of possible high frequency currents through the PV array's stay capacitance to earth ground. Conventional PV inverters also typically utilize electrolytic capacitors for bulk power buffering. However such capacitors can be prone to decreased reliability.

The solution proposed here to solve these problems is a bi-directional buck boost converter combined with half bridge inverters. This configuration enables grounding of the array's negative terminal and passive power decoupling with only film capacitors.

Several aspects of the proposed converter are discussed. First a literature review is presented on the issues to be addressed. The proposed circuit is then presented and examined in detail. This includes theory of operation, component selection, and control systems. An efficiency analysis is also conducted. Simulation results are then presented that show correct functionality. A hardware prototype is built and experiment results also prove the concept. Finally some further developments are mentioned.

As a summary of the research a new topology and control technique were developed. The resultant circuit is a high performance transformerless PV inverter with upwards of 97% efficiency.

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$\omega$ Grid frequency (rad/s)

$\phi$ Grid current displacement angle, relative to voltage

$\Theta$ Instantaneous grid voltage angle ($\omega t$)

$\gamma$ Steinmetz constant

$\alpha$ Steinmetz constant

$A$ Cross sectional area of core ($cm^2$)

$A_l$ Inductance factor

$AC$ Alternating Current

$\beta$ Steinmetz constant

$B$ Time varying flux density (Gauss)

$\hat{B}$ Peak flux density (Gauss)

$\Delta B$ Peak to peak flux density (Gauss)

$C_{gs}$ Gate to source capacitance

$C_{gd}$ Gate to drane (Miller) capacitance

$C_{ds}$ Drane to source capacitance

$C_C$ Thermal capacitance of transistor case

$C_S$ Thermal capacitance of heat sink

$d$ Time varying duty ratio

$d_1$ Time varying duty ratio of buck boost converter

$D_1$ Steady state duty ratio of buck boost converter

$d_2$ Time varying duty ratio of line 1 inverter

$D_2$ Steady state duty ratio of line 1 inverter

$d_3$ Time varying duty ratio of line 2 inverter

$D_3$ Steady state duty ratio of line 2 inverter

$DC$ Direct Current

$DSP$ Digital Signal Processor

$E_{on}$ Turn-on transition energy

$E_{off}$ Turn-off transition energy

$E_{tot}$ Sum of turn on and turn off transition energy

$E_{diode}$ Reverse recovery energy of diode

$E_{drive}$ Energy dissipated in driver circuit

$f_{sw}$ Switching frequency ($Hz$)

$f_{eq}$ Equivelant frequency

$I_{inv}$ Net average current drawn by inverter on DC link

$I_g$ Grid current magnitude

$I_{g\_rms}$ Grid RMS current

$i_1$ Time varying average current of $L_1$

$I_1$ Steady state average current of $L_1$

$I_{1\_rms}$ Root mean square current through $L_1$

$\Delta I_1$ Peak-peak switching frequency current ripple through $L_1$

$i_2$ Time varying average current of $L_2$

$I_2$ Steady state average current magnitude of $L_2$

$\Delta I_2$ Peak-peak switching frequency current ripple through $L_2$

$i_3$ Time varying average current of $L_3$

$I_3$ Steady state average current magnitude of $L_3$

$\Delta I_3$ Peak-peak switching frequency current ripple through $L_3$

$i_4$ Input current from PV array

$i_{pv}$ Input current from PV array

$i_5$ Disturbance current associated with positive DC link

$i_6$ Disturbance current associated with negative DC link

$i_{Q1}$ Time varying current through transistor $Q_1$

$i_{Q1\_rms}$ RMS current through transistor $Q_1$

$i_{Q2}$ Time varying current through transistor $Q_2$

$i_{Q2\_rms}$ RMS current through transistor $Q_2$

$i_{Q3}$ Time varying current through transistor $Q_3$

$i_{Q3\_rms}$ RMS current through transistor $Q_3$

$I_{Q3\_on}$ Current through $Q_3$ instant after switch on

$I_{Q3\_off}$ Current through $Q_3$ instant before switch off

$i_{Q4}$ Time varying current through transistor $Q_4$

$i_{Q4\_rms}$ RMS current through transistor $Q_4$

$I_{Q4\_on}$ Current through $Q_4$ instant after switch on

$I_{Q4\_off}$ Current through $Q_4$ instant before switch off

$I_{gate}$ Instantaneous gate current

$K_1$ Control system for buck boost converter

$K_2$ Control system for grid current

$K_3$ Control system for regulating average voltage across $C_1$

$k$ Arbitrary constant

$MPPT$ Maximum Power Point Tracking

$MOSFET$ Metal Oxide Semiconductor Field Effect Transistor

$M$ Modulating index

$N$ Number of turns

$\eta$ Efficiency

$p_{pv}$ Instantaneous input (PV) power

$p_g$ Instantaneous grid power

$P_{Q\_cond}$ Average conduction loss (one transistor)

$P_{Q\_sw}$ Average switching loss (one transistor)

$P_1$ Linear buck boost converter plant

$P_2$ Linear inverter current plant

$P_3$ Linear energy balance plant

$P_{in}$ Average input power

$P_{diss}$ Average total power dissipated in converter

$P_{L1}$ Average power dissipated in $L_1$

$P_{L2}$ Average power dissipated in $L_2$

$P_{L3}$ Average power dissipated in $L_3$

$P_{Q1}$ Average power dissipated in $Q_1$

$P_{Q2}$ Average power dissipated in $Q_2$

$P_{Q3}$ Average power dissipated in $Q_3$

$P_{Q4}$ Average power dissipated in $Q_4$

$P_{Q5}$ Average power dissipated in $Q_5$

$P_{Q6}$ Average power dissipated in $Q_6$

$P_{L\_cop}$ Power dissipated in an inductor copper wire

$P_{L\_core}$ Power dissipated in an inductor magnetic core

$p_{C1}$ Instantaneous power absorbed or supplied by $C_1$

$P_v$ Core loss (power per unit volume)

$PV$ Photovoltaic

$PWM$ Pulse Width Modulation

$Q_c$ Reverse recovery charge of diode

$Q_{gs}$ Gate to source charge

$Q_{gd}$ Gate to drane charge

$Q_r$ Reverse recovery charge of body diode

$Q_g$ Total gate charge

$R_{ds}$ On state resistance of MOSFET

$R_g$ Total gate resistance

$R_{JC}$ Thermal resistance of junction to case

$R_{SA}$ Thermal resistance of heat sink to ambient

$R_{CS}$ Thermal resistance of insulating pad (case to heat sink)

$RMS$ Root Mean Square

$SiC$ Silicon carbide

$SBD$ Schottky Barrier Diode

$T_{sw}$ Switching period ($s$)

$t_{ri}$ Current rise time

$t_{fi}$ Current fall time

$t_{rv}$ Voltage rise time

$t_{fv}$ Voltage fall time

$T_j$ Junction temperature

$T$ Period (s)

$TI$ Texas Instruments

$US$ United States

$V_g^+$ Gate driver positive voltage

$V_g^-$ Gate driver negative voltage

$V_g$ Split phase grid voltage magnitude

$V_{g\_rms}$ Split phase RMS grid voltage

$V_{g\_1\phi}$ Single phase grid voltage magnitude

$V_{g\_rms\_1\phi}$ Single phase RMS grid voltage

$v_g$ Time varying grid voltage

$v_1$ Time varying average voltage of $C_1$

$V_1$ Steady state average voltage of $C_1$

$V_{1r}$ Ripple voltage magnitude of $v_1$

$v_2$ Time varying average voltage of $C_2$

$V_2$ Steady state average voltage of $C_2$

$\Delta V_2$ High frequency peak-peak ripple voltage of $v_2$

$V_{plat}$ Platteau voltage

$V_f$ On-state voltage drop of diode

$V_{drive}$ Instantaneous driver voltage

$V_{Q3\_on}$ Voltage across $Q_3$ instant before switch on

$V_{Q3\_off}$ Voltage across $Q_3$ instant after switch off

$V_{Q4\_on}$ Voltage across $Q_4$ instant before switch on

$V_{Q4\_off}$ Voltage across $Q_4$ instant after switch off

$V_{ds}$ Drane to source voltage

$V_{on}$ Voltage applied across coil

$v_5$ Instantaneous line 1 grid voltage

$v_6$ Instantaneous line 2 grid voltage

$ZVS$ Zero Voltage Switching

# Chapter 1

# INTRODUCTION

Presented here is a study of a novel transformerless inverter that utilizes only film type capacitors. The objective is to create an improved power inverter circuit. In [1] the inverter is identified as the least reliable component of a PV array system. In [2] reliable capacitors and transformerless topologies are identified as "examples of opportunities that will contribute to cost and performance improvements."

The new inverter topology is evaluated analytically, in simulation, and with hardware at various time scales. First some background is presented on transformerless inverters and power decoupling in context of single phase PV array inverters. The proposed converter functionality is discussed along with some criteria for selecting components. A control system is then developed to meet operating and performance objectives. An analytic prediction of efficiency is also presented. The design is then thoroughly validated in simulation. Finally a prototype is constructed and tested to prove the concept. Results show the proposed circuit is a viable solution.

## 1.1 Background

Solar electric systems have become more popular in recent years [3]. Lower purchase cost and improved reliability are important design objectives for greater acceptance into the market.

Reduced cost may be accomplished with simple circuitry. Transformerless type inverters result in reduced size, complexity, and weight along with improved efficiency. According to [4], transformerless topologies are on average about $2\%$ more efficient. Safety codes for PV inverters have been modified in the US to permit such inverters provided that they include certain protection features [5]. However transformerless inverters are not trivial circuits to implement because of possible leakage ground currents through the PV panels.

Improved reliability (long term value) is also beneficial to the customer and manufacturer. Inverter reliability may be improved through the use of film type capacitors. However this is not always possible in single phase inverters because of power decoupling requirements. This research attempts to address both the transformerless inverter ground currents and power decoupling issues.

### 1.1.1 Single Phase Transformerless PV Inverters

Single phase inverters can have problems associated with high frequency leakage currents through the array's stray capacitance to earth ground. A typical H-bridge power inverter is illustrated in

Figure 1.1. The PV array is depicted as a DC voltage source and the stray capacitances of the array to earth are also shown. Instantaneous switching states are depicted in Figure 1.2 for the H-bridge inverter operating with uni-polar modulation in the positive half cycle. It can be seen the array's positive and negative terminals are alternately switched to earth potential; this leads to dangerous currents through the stray capacitance of the PV array. Eliminating these currents is a design objective of transformerless inverters.

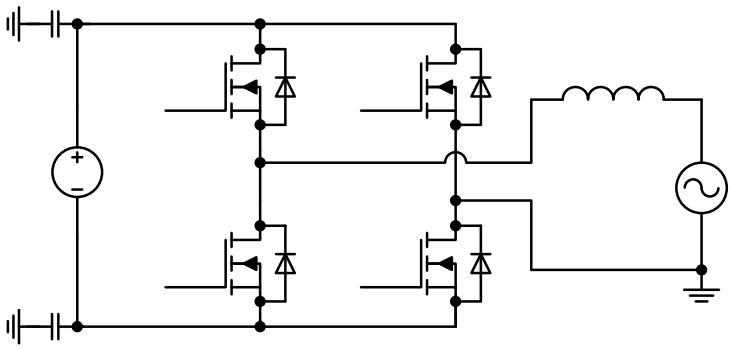

Figure 1.1: H-bridge Power Inverter

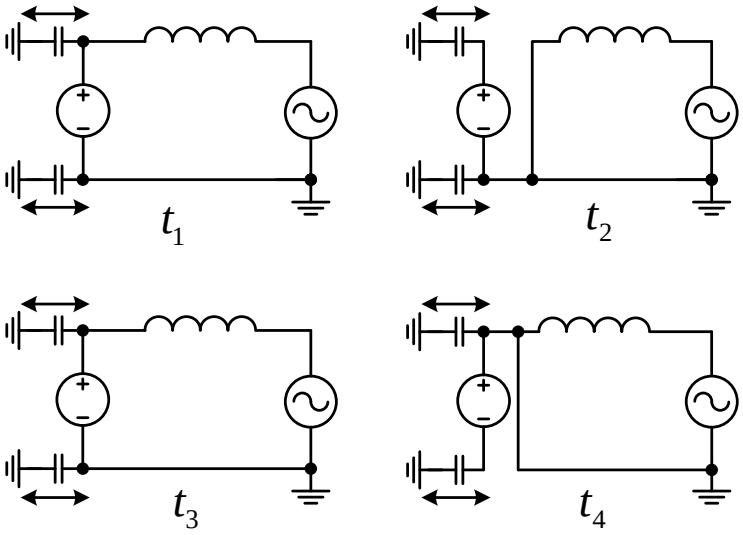


Figure 1.2: H-bridge Inverter Unipolar Modulation Switching States

### 1.1.2 Single Phase Inverter Power Decoupling

Another important aspect of single phase inverters is decoupling the instantaneous input and output power. A black box depiction of such an inverter is shown in Figure 1.3 with the grid voltage and

current given by (1.1) and (1.2) respectively. Losses are assumed negligible for this discussion.

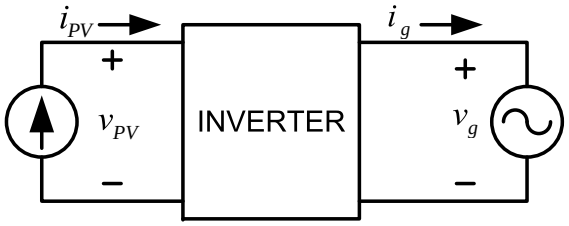


Figure 1.3: Inverter as a Black Box

$$v_g(t) = V_g \cos(\omega t) \tag{1.1}$$

$$i_g(t) = I_g \cos(\omega t + \phi) \tag{1.2}$$

Instantaneous power fed to the grid should include both constant and oscillating terms (1.3). Figure 1.4 illustrates the average and oscillating components of power fed to the grid.

$$p_g(t) = \frac{V_g I_g \cos(\phi)}{2} + \frac{V_g I_g \cos(2\omega t + \phi)}{2} \tag{1.3}$$

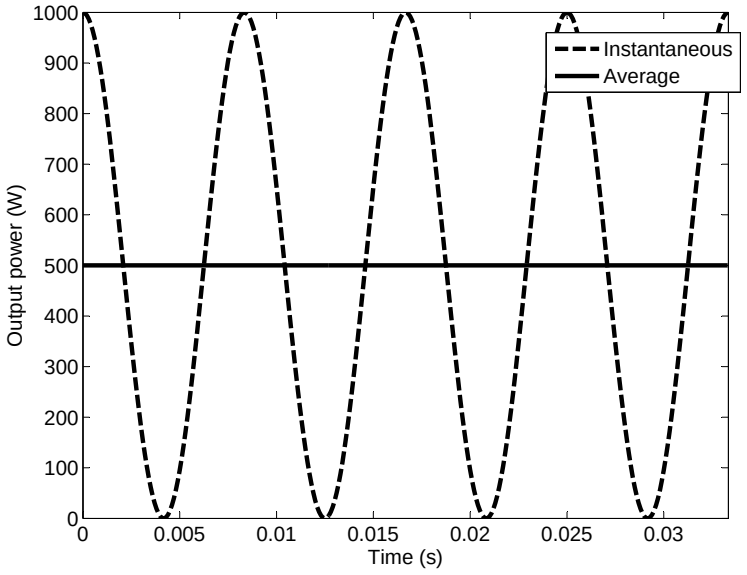


Figure 1.4: Average and Instantaneous Power Delivered to Grid

Instantaneous power drawn from the array should be constant for efficient Maximum Power Point Tracking (MPPT). The array's input voltage will be regulated essentially constant at the maximum

power point and so the input current should also be constant. Figure 1.5 illustrates the desired instantaneous input power waveform.

$$p_{pv}(t) = v_{pv} i_{pv} = k \tag{1.4}$$

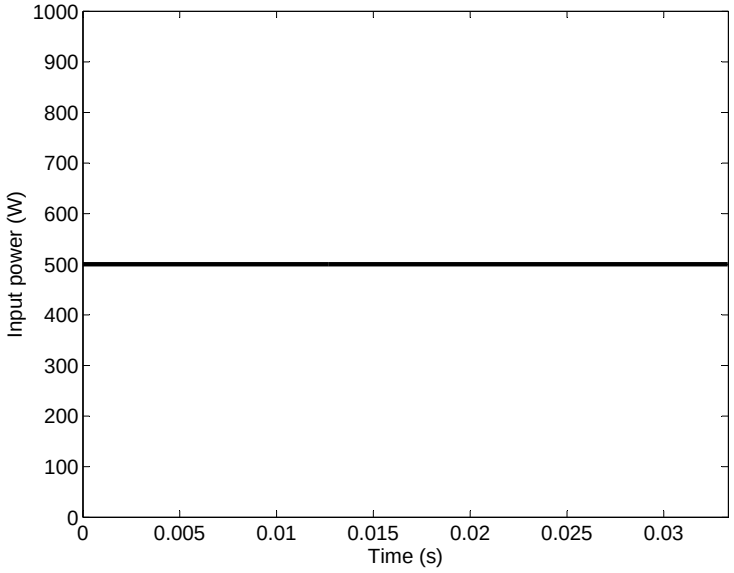


Figure 1.5: Desired Instantaneous Power from PV Array

An energy buffer is required to absorb the double line frequency component of (1.3). Typically large electrolytic capacitors are utilized for this purpose. However the electrolyte within these capacitors may evaporate over time leading to reduced reliability, especially at elevated temperatures. It is thus desirable to decouple the oscillating power of single phase inverters with energy storage elements other than electrolytic capacitors.

## 1.2 Literature Review

A sufficient literature review was conducted. This mostly included topics from transformerless topologies and power decoupling of inverters.

### 1.2.1 Single Phase Transformerless PV Inverters

As previously mentioned, a practical transformerless PV inverter must avoid high frequency, common mode, ground currents through the PV array's stray capacitance to earth ground. Such currents

can be reduced with a large common mode filter; although in this discussion other solutions will be evaluated.

Many circuits have been developed to mitigate such stray currents. Some solutions directly connect the PV negative terminal to earth through the inverter. Other circuits have only DC or low frequency AC potential of the array relative to earth ground. The best solutions have little or no stray currents while maintaining high efficiency and low cost. A review of some past research on this topic is presented in [4] [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], and [17].

Before listing the common transformerless inverters, it is important to note that this is not necessarily a side by side comparison, just a topology review. Some inverters require an additional boost converter and some do not. Also different countries have different residential grid voltage configurations.

The half bridge (two level) inverter is probably the simplest solution. This circuit is not necessarily the most efficient though. Figure 1.6 shows an example of a half bridge inverter. In such a circuit, the PV array is at DC potential relative to earth. The multi-level variation of the half bridge inverter [18], [19], and [20], illustrated in Figure 1.7, is more efficient yet more expensive.

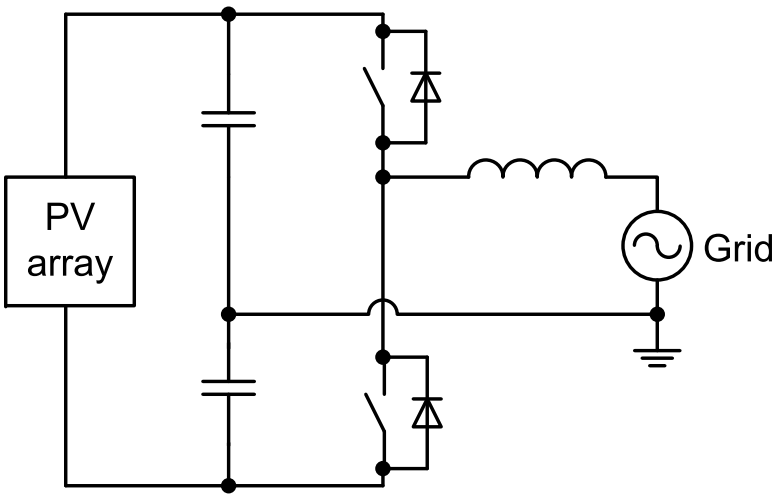


Figure 1.6: Half Bridge Inverter

It is also possible to eliminate ground currents by directly connecting the negative PV terminal to earth ground. Such circuits are sometimes referred to as double grounded inverters. The simplest double grounded inverter is the half bridge inverter with generation control as mentioned in [9] and [21]. This topology illustrated in Figure 1.8 requires two PV arrays to maintain a sufficient potential and balance on the net DC link. Another double grounded transformerless inverter is the Karschny inverter [22] illustrated

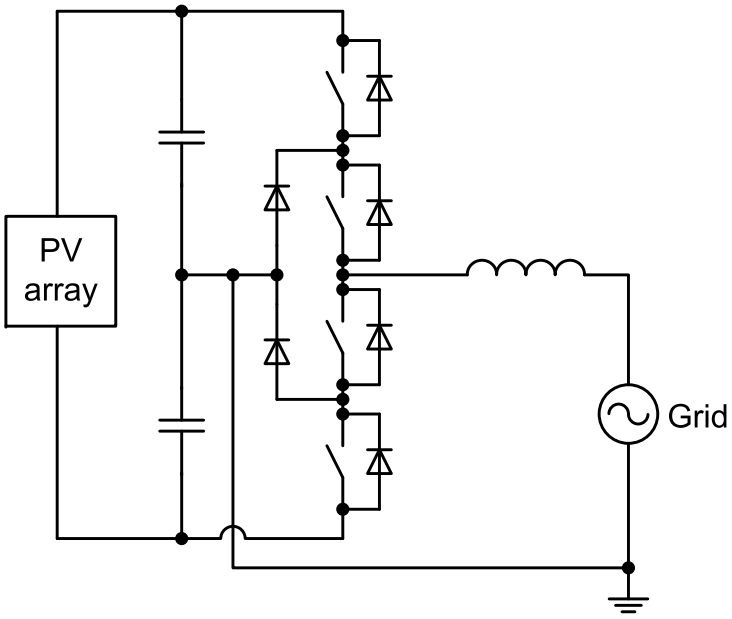


Figure 1.7: Three Level Version of Half Bridge

in Figure 1.9. Other double grounded inverters are listed in reference [23].

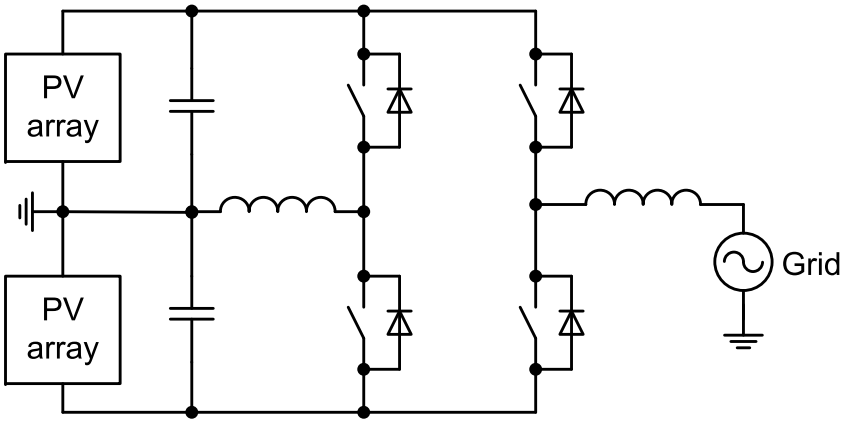


Figure 1.8: Half Bridge Inverter with Bi-directional Buck Boost Converter and Generation Control

Variations of the H-bridge inverter with uni-polar modulation are more common. These circuits are popular because the three voltage levels lead to reduced inductor requirements and improved efficiency. The HERIC [24], and the H5 [25] inverters are such solutions that require additional semiconductors to provide alternative freewheeling current paths. The HERIC topology of Figure 1.10, provides an alternative current path at the grid side during zero voltage instants. This enables switching off the

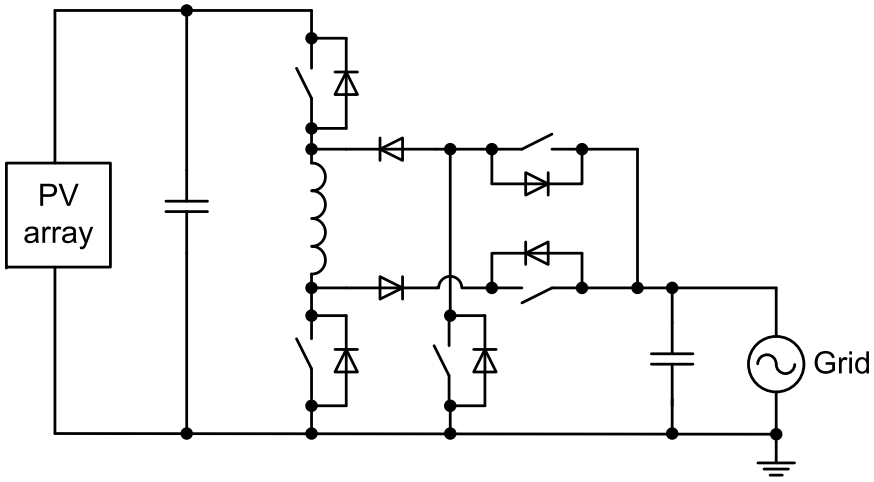


Figure 1.9: Double Grounded Karschny Inverter

entire H-bridge during the zero state which greatly reduces leakage currents through the array. Another protected topology is the H5 inverter of Figure 1.11. The top two transistors of the H-bridge are utilized for the zero state. The extra switch at the input to the bridge is switched off during the zero state to reduce ground currents. The H-bridge variations are discussed in more detail along with an efficiency summary in [8].

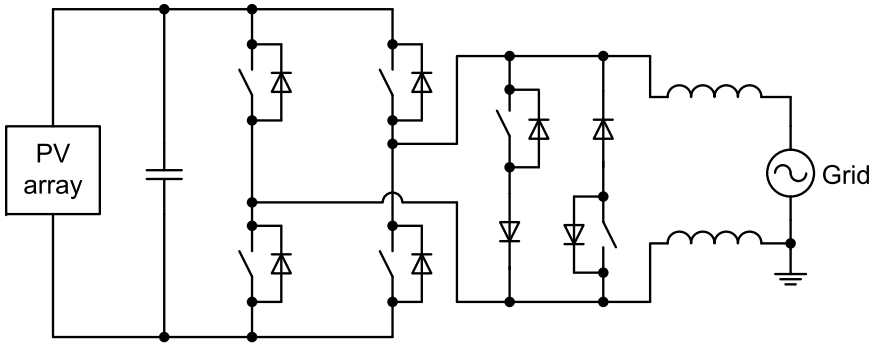


Figure 1.10: HERIC Inverter

Other variations of the H-bridge are illustrated here. The H6 with AC bypass [26] is shown in Figure 1.12. The H6 with DC bypass [11] is shown in Figure 1.13. Other H6 variations are reported in [17]. The full bridge with DC bypass [7] is illustrated in Figure 1.14.

A few more interesting transformerless circuits are shown here. The “virtual DC bus” [13], illustrated in Figure 1.15, is a flying capacitor type of circuit and is also double grounded. A dual buck converter circuit is described in [27] and illustrated in Figure 1.16. This circuit has two separate step

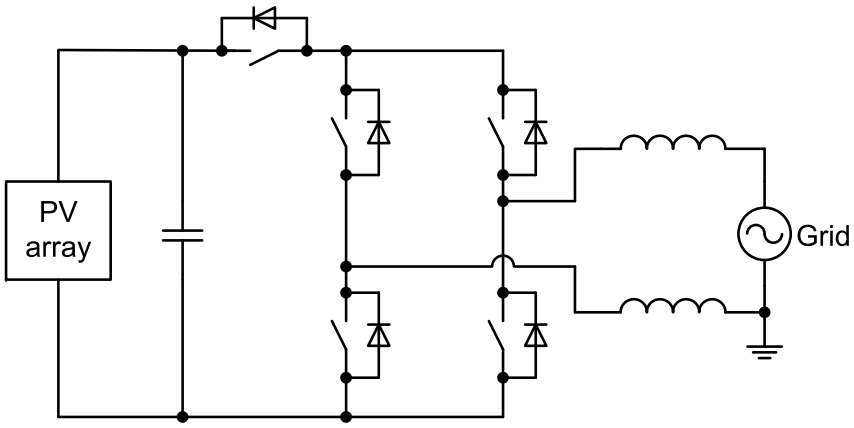


Figure 1.11: H5 Inverter

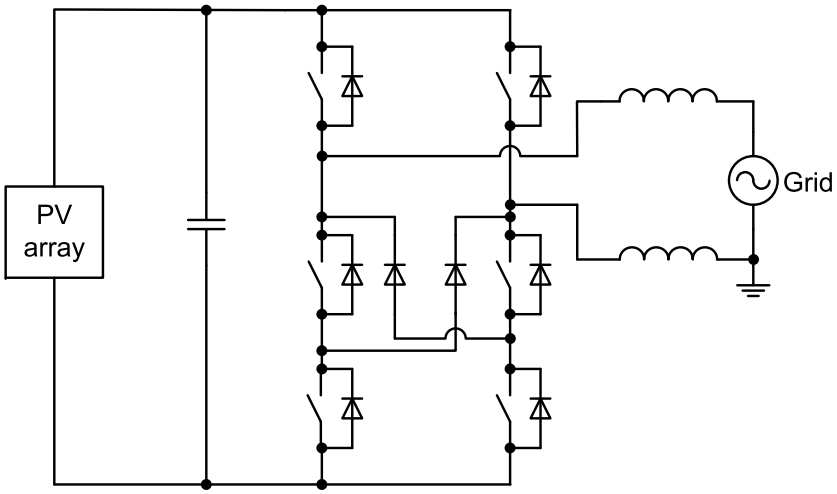


Figure 1.12: H6 Inverter with AC Bypass

down converters to regulate current in each half of the wave. A current source transformerless inverter is discussed in [28]. Reference [29] proposes an interesting circuit to establish a net DC link.

### 1.2.2 Single Phase Inverter Power Decoupling

Reference [30] presents a summary of various approaches to power buffering in single phase PV inverter applications. Power decoupling is categorized based upon where the decoupling circuit is placed within the converter. This may be at the PV side, on the DC link (for multi-stage converters), or at the AC side of the converter.

A basic parallel active power filter on the PV side is illustrated in Figure 1.17 and described

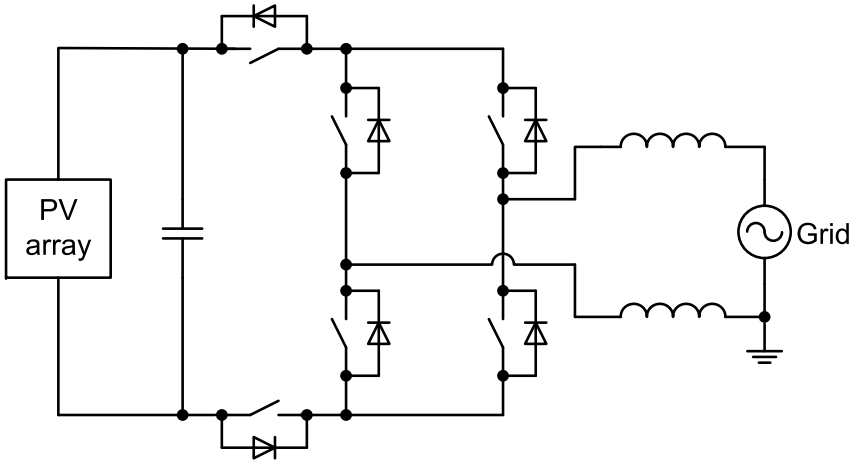


Figure 1.13: H6 Inverter with DC Bypass Inverter

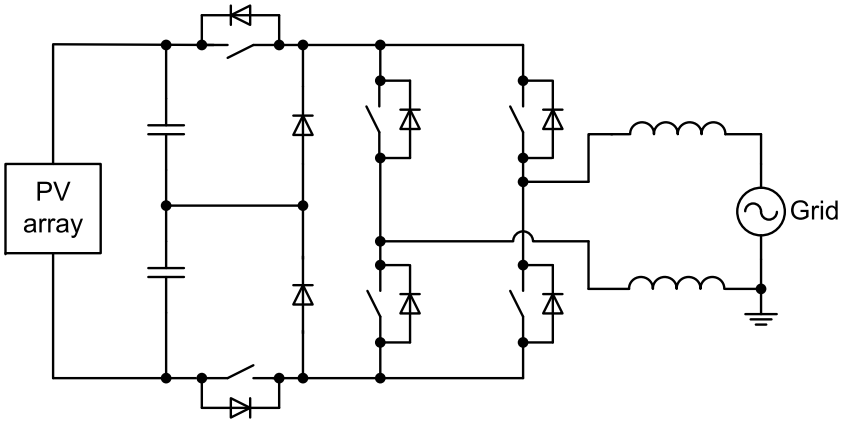


Figure 1.14: Full Bridge with DC Bypass

in [31], [32], and [33]. Here instantaneous current is regulated through a separate converter such that there is essentially no current or voltage ripple seen by the PV array. This approach is effective yet has drawbacks such as increased cost and reduced overall efficiency. This type of power buffer could also be placed across the DC link of a multi-stage converter, or connected through a multi-port transformer [34]. Reference [35] also describes power decoupling on the DC link.

Furthermore as reported in [36] and [37], active power decoupling may also be implemented on the AC side. This method is similar in concept to the parallel active filters previously discussed although more complicated because of AC currents and voltages.

Another power decoupling technique is to permit a large double line frequency voltage ripple

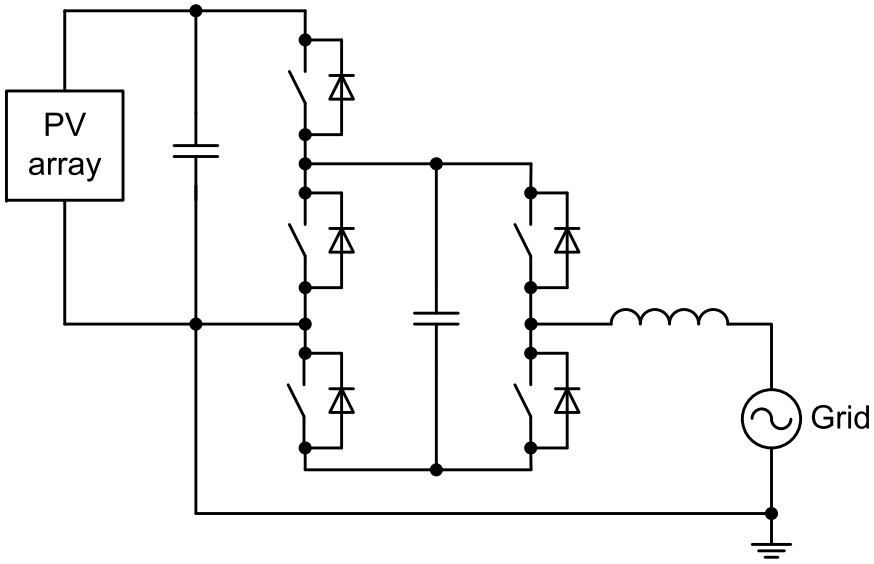


Figure 1.15: Virtual DC Link Transformerless Inverter

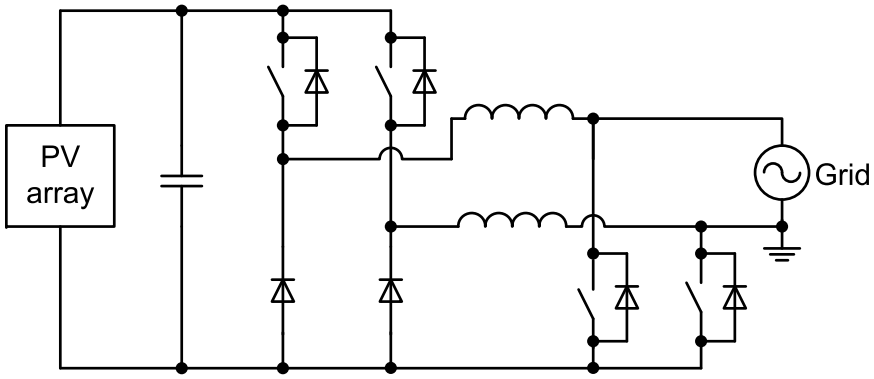


Figure 1.16: Dual Buck Converter Inverter

across the DC link capacitor [38]. This is considered a passive approach. For a given current ripple to be absorbed ($i_c$), a larger voltage ripple ($v_c$) will allow a reduced size link capacitor according to (1.5). However slight modifications to the inverter control loop are necessary to avoid grid current distortions [30], [38], and [39].

$$C = i_c \frac{dt}{dv_c} \tag{1.5}$$

## 1.3 Proposed Power Circuit

The proposed converter of this study is illustrated in Figure 1.18. This circuit is a combination of a bi-directional buck-boost converter and two half-bridge inverters [40]. The PV array is represented by the current source $i_4$.

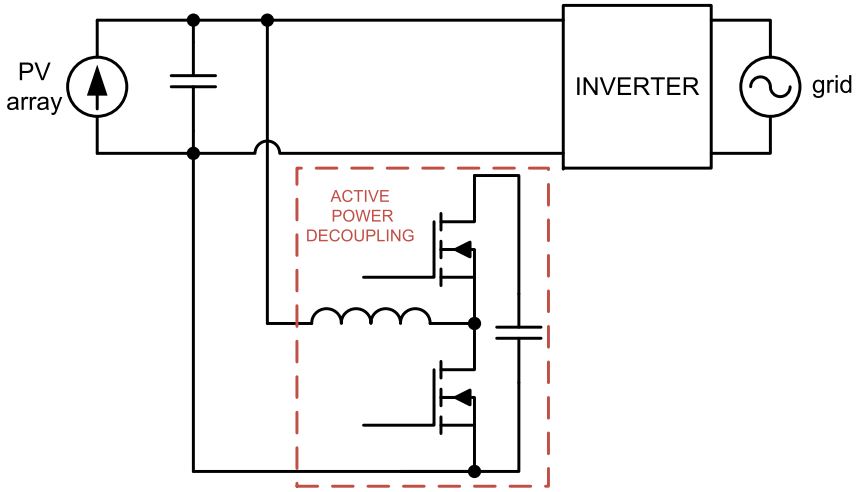


Figure 1.17: Parallel Active Power Decoupling

This inverter would supply a split phase circuit that is comprised of two $120\ VRMS$ (relative to earth ground) lines that are $180°$ out of phase. Also this version would work with a series connected PV array such that the minimum input operating voltage is about $200\ VDC$ and the maximum (open circuit) input voltage is about $550\ VDC$.

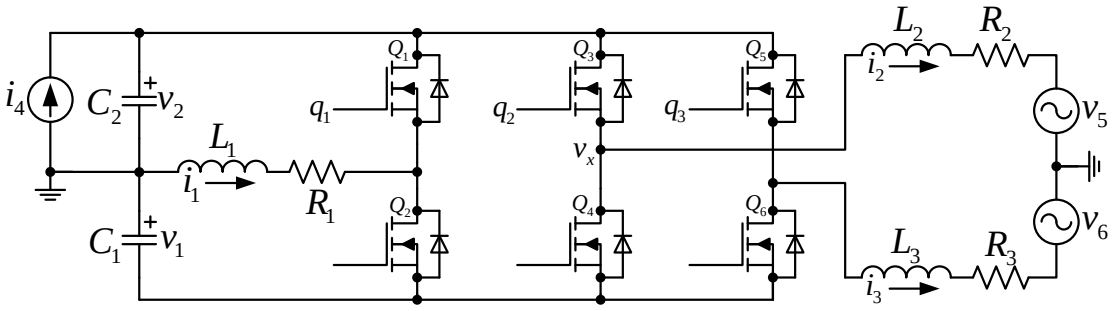


Figure 1.18: Split Phase Version of Proposed Topology

The inverter would be wired as an ungrounded array; although the PV array's negative terminal would be at earth potential through the neutral line of the inverter. This essentially eliminates the possibility of ground currents. However NEC and IEC requirements for transformerless, ungrounded systems would have to be satisfied; this includes a Ground Fault Detector Interrupter (GFDI) [41].

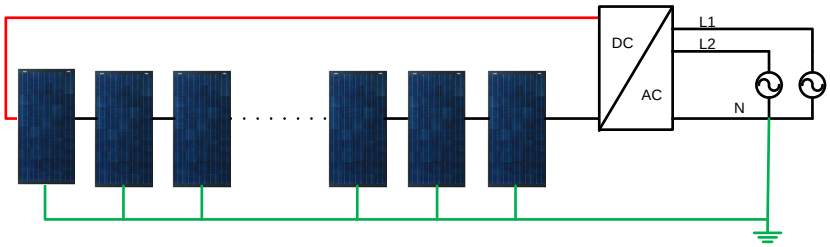


Figure 1.19: Wiring Configuration for Ungrounded PV String Inverter

### 1.3.1 Theory of Operation

From an average system perspective the buck-boost converter is responsible for regulating the input voltage $(v_2)$ constant. The buck boost converter also establishes a net DC link that is at most twice the input voltage. Furthermore the bi-directional capability of the buck boost converter enables the bottom side capacitor $(C_1)$ to buffer grid power pulsations. Since $C_1$ is completely decoupled from the PV array, a large voltage ripple may be permitted across this capacitor leading to reduced capacitance requirement. Under normal operation the average voltage across $C_1$ will be regulated constant to maintain energy balance while allowing significant (double line frequency) voltage swings. This power decoupling configuration enables tight regulation of the input voltage $(v_2)$ for efficient MPPT [42].

This topology is built upon past research. Specifically the concept of establishing the net DC link with the buck boost converter is borrowed from [43] and [44]. These circuits utilize a uni-directional buck-boost converter with no consideration of power decoupling. The bi-directional buck boost converter is borrowed from reference [21] and [45] where it is used for balancing under partial shaded conditions. An example of power decoupling by permitting large voltage swings on the DC link capacitor is discussed in [38].

This circuit solves the challenges of ground currents and power decoupling in a simple manner. Also this circuit does not require additional semiconductors of typical transformerless inverters because the negative terminal of the PV array is at ground potential. Inefficient active power decoupling is not necessary because the power buffer capacitor is separate from the PV array.

### 1.3.2 Other Variations

Other arrangements of the proposed topology are also possible. The single phase version of Figure 1.20 is essentially the same. The three phase version is similar to the circuit proposed in [43] and

is capable of low frequency power decoupling in the case of unbalanced grid conditions.

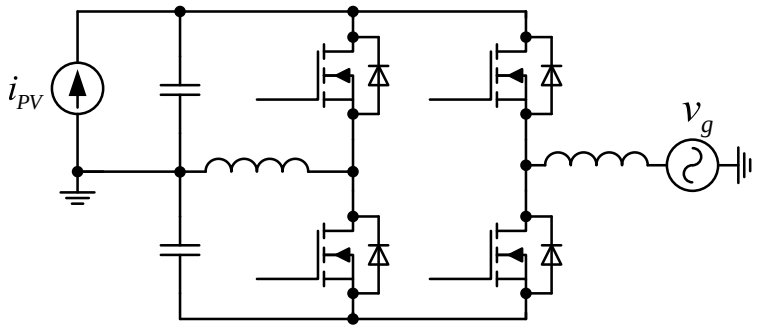


Figure 1.20: Single Phase Version of Proposed Topology

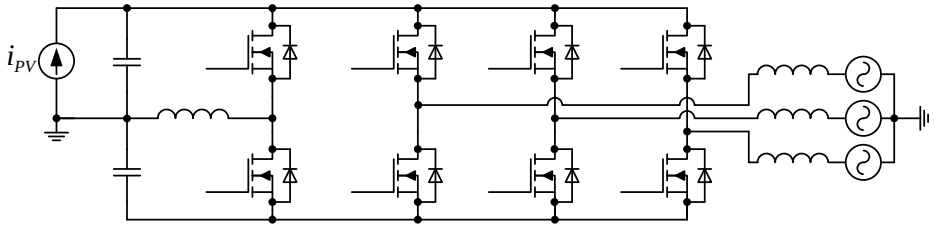


Figure 1.21: Three Phase Version of Proposed Topology

### 1.3.3 Neutral Currents

This split phase version is capable of supplying neutral currents (unbalanced AC network) if necessary. However it is desirable to keep the neutral current zero. The inverter section, as illustrated in Figure 1.18, can actually be considered as two separate converters because each power pole has a separate path to neutral. High frequency neutral currents can be canceled by phase shifting the Pulse Width Modulation (PWM) carrier signals of the half bridge inverters by $180°$. The magnitude of the waveforms in the following image are unitless.

A simulation was conducted to show this; instantaneous waveforms are shown in Figure 1.23 at the peak of the current wave. The PWM signals for the top side transistors of each half bridge inverter are shown along with instantaneous inductor currents. The neutral current is shown in the bottom trace.

Low frequency neutral current is also illustrated in Figure 1.24 at startup and in presence of an unbalanced current reference step at .1 seconds. Under normal operation, the neutral current is zero.

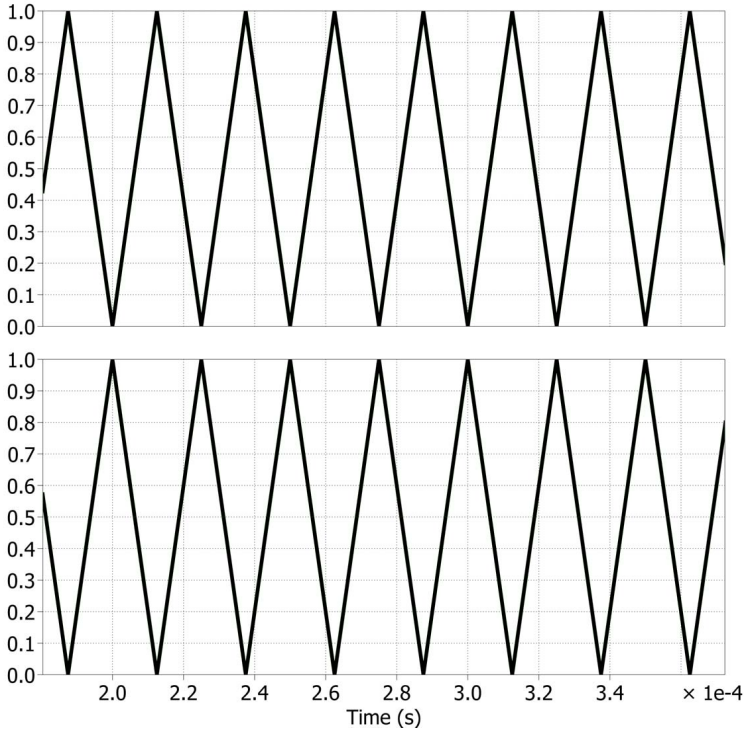


Figure 1.22: PWM Carrier Waveforms for Split Phase Inverter

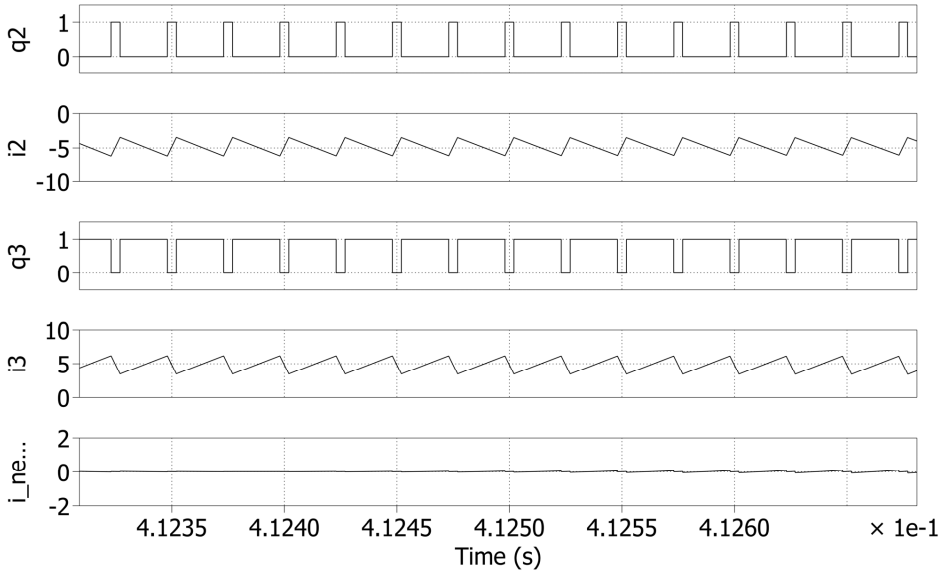


Figure 1.23: High Frequency Inductor and Neutral Currents

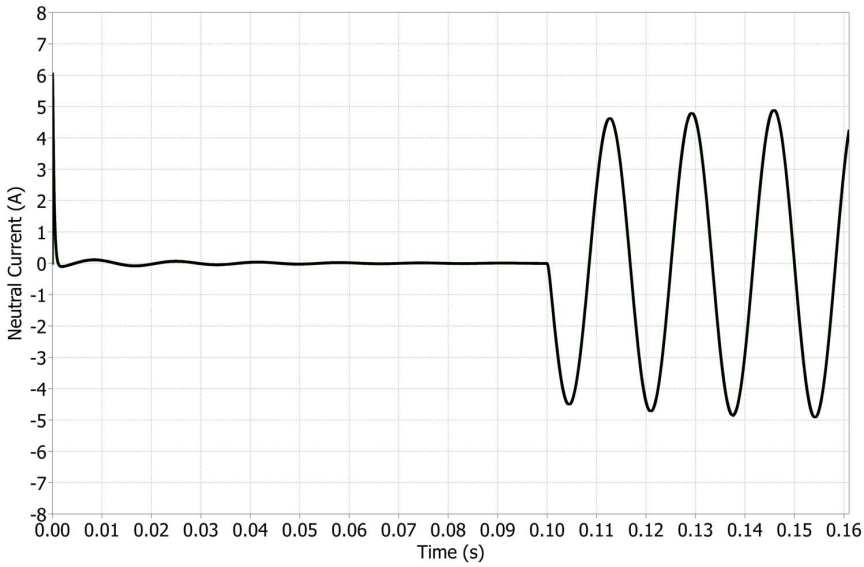


Figure 1.24: Neutral Current of Split Phase Inverter at Start Up and Unbalanced Operation

Chapter 2

# ENERGY STORAGE COMPONENTS

Identifying appropriate components is an important aspect of hardware design and concept validation. Some basic guidelines are presented here to select the power inductors and capacitors of the proposed transformerless inverter. The converter to be built is illustrated again along with stray resistances, reference designators, and average state variable definitions.

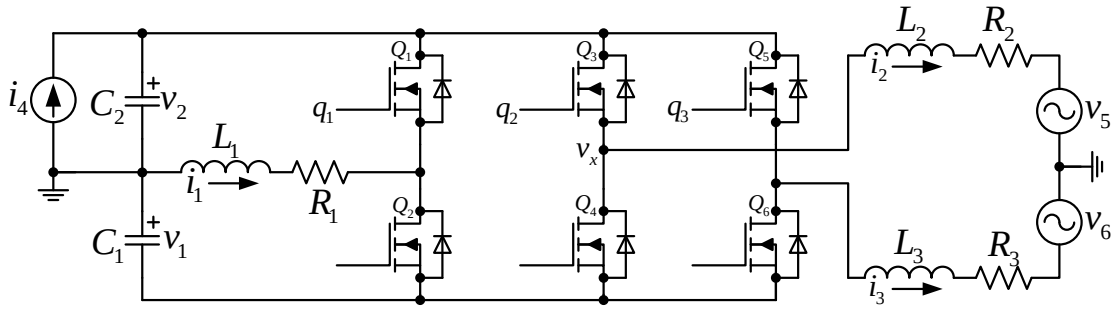


Figure 2.1: Power Circuit Prototype with Reference Designators

## 2.1 Buck Boost Inductor ($L_1$)

A first approach to calculating the buck boost inductance is with the permitted ripple current. The inductor current peak-peak ripple magnitude $(\Delta I_1)$ can be written in terms of both capacitor voltages, switching frequency, and inductance. The voltages here are the average, constant approximations.

$$\Delta I_1 = \frac{V_1 V_2}{(V_1 + V_2) f_{sw} L_1} \tag{2.1}$$

For a fixed inductance, this equation is illustrated in Figure 2.2 at $40\ kHz$ switching frequency. The worst case occurs when both DC link capacitors are at maximum voltage.

With (2.1), the inductance can be found as a function of permitted peak to peak ripple current. As an example, with a peak-peak ripple current of $14\,A$ and maximum input voltage of $550\,V$, an inductance of about $500\,uH$ is required.

Furthermore the inductance has an effect on the poles of the system. For control design purposes discussed later, it is desirable to locate the system resonance below the open loop crossover. Figure 2.3 shows the transfer characteristics of $d_1$ to $v_2$ and how increased inductance results in reduced resonant frequency.

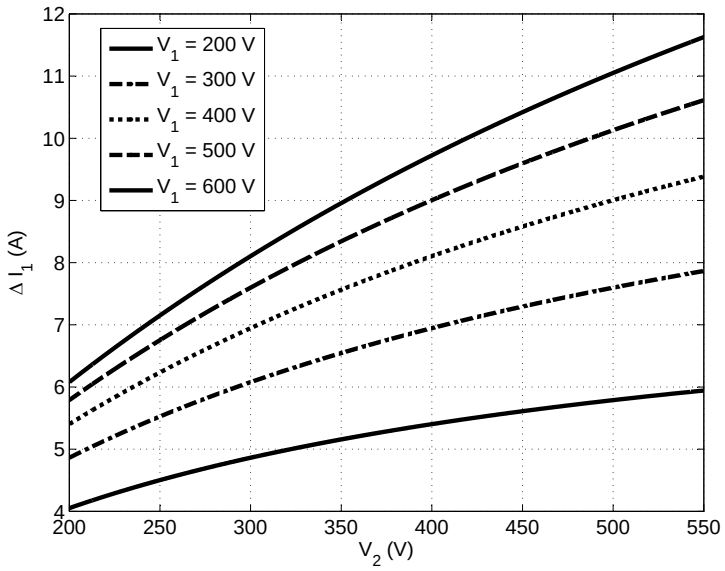


Figure 2.2: Buck Boost Inductor Current Ripple at Several Voltages

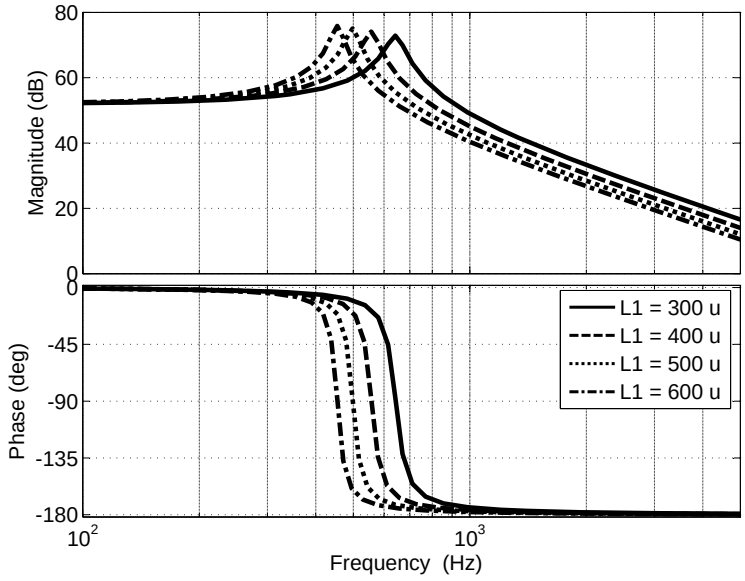


Figure 2.3: The Effect of Buck Boost Inductance on Frequency Response ($d_1$ to $v_2$)

Also the peak flux density is a parameter to consider when selecting this inductor. Later in the efficiency section, it is shown that core losses are very much a function of flux density. Increasing the inductance results in reduced peak flux density and reduced core losses.

## 2.2 Bottom Side Capacitor ($C_1$)

There are several conflicting objectives when selecting the bottom side capacitance. A small capacitance is desirable such that a film capacitor may be utilized. However the capacitor cannot be made too small because it must absorb the double line frequency power ripple without excessive voltage swings. Some trade-offs are discussed. It is assumed only the double line frequency ripple current is present.

The capacitor voltage can be written in terms of average $(V_1)$ and low frequency ripple magnitude $(V_{1r})$ components.

$$v_1(t) = V_1 + V_{1r}\sin(2\omega t) \tag{2.2}$$

The capacitor voltage squared includes both constant and time varying components:

$$v_1^2(t) = V_1^2 + 2V_1V_{1r}\sin(2\omega t) + \frac{V_{1r}^2}{2} - \frac{V_{1r}^2}{2}\cos(4\omega t) \tag{2.3}$$

The capacitor voltage squared can also be found by first equating the capacitor's instantaneous power to the grid instantaneous power ripple (1.3). Here the grid voltage ($V_g$) is actually twice the voltage of each phase leg (equivalent to a single phase circuit).

$$p_{C_1}(t) = \frac{d}{dt}\left(\frac{1}{2}C_1v_1^2(t)\right) = \frac{V_gI_g\cos(2\omega t)}{2} \tag{2.4}$$

Integrating then gives another expression for the capacitor voltage squared.

$$v_1^2(t) = \frac{V_gI_g}{2\omega C_1}\sin(2\omega t) \tag{2.5}$$

Equating the magnitude of the double line frequency component from (2.3) to the magnitude of (2.5) gives the capacitance in terms of the average capacitor voltage, capacitor voltage ripple magnitude, and grid voltage/current magnitudes. This equation was verified to be correct in both experiment and simulation.

$$C_1 = \frac{V_gI_g}{4\omega V_1V_{1r}} \tag{2.6}$$

Equation (2.6) is illustrated in Figure 2.4 for several average voltage conditions at the maximum output power of $1\ kVA$. Increasing the average $(V_1)$ or ripple $(V_{1r})$ components results in reduced capacitance requirements. These plots may be used to select a capacitance for the bottom side DC link. Reference [38] states a ripple of up to $25\%$ is possible without causing grid current distortion. This was

verified to be true in simulation when the average capacitor voltage is only slightly greater than the peak grid voltage.

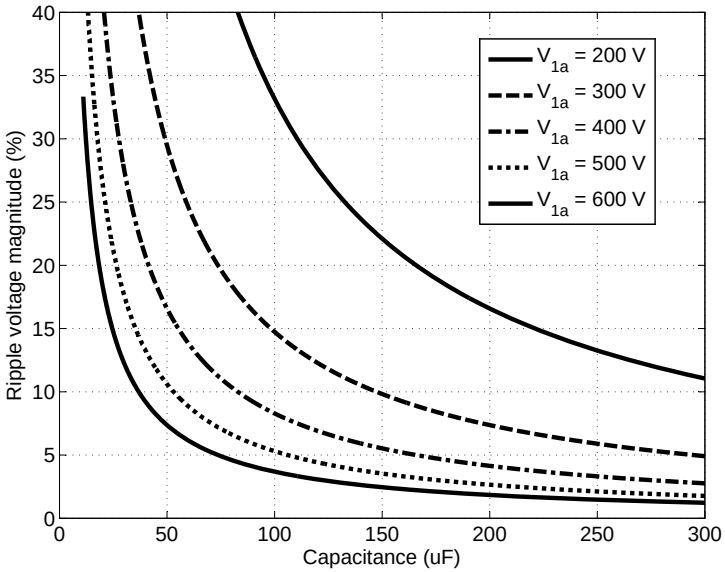


Figure 2.4: $C_1$ Ripple Magnitude as Percentage of Average Voltage

Since the bottom side capacitor is decoupled from the input, its average voltage may be set arbitrarily or scheduled. This is an aspect that may be studied in more detail. A greater average voltage permits more voltage ripple and smaller capacitance requirement. However the average voltage cannot be increased too much because this increases switching and inductor losses and also may result in excessive voltages across the transistors. Also the capacitance cannot be reduced too much because of transient behaviour at start up. An optimum solution may exist.

The capacitor should also have sufficient current carrying capacity. The low frequency average capacitor ripple current can be found by first combining (2.2) and (2.6) to attain an expression for the capacitor's time varying ripple voltage. The current is then the first derivative of the voltage multiplied by the capacitance.

$$v_{1r}(t) = \frac{V_g I_g}{4C_1 \omega V_1} sin(2\omega t) \tag{2.7}$$

$$i_{C1}(t) = C_1 \frac{dv_{1r}}{dt} = \frac{V_g I_g}{2V_1} \cos(2\omega t) \tag{2.8}$$

## 2.3 Top Side Capacitor ($C_2$)

The top side capacitor ($C_2$) must only absorb high frequency ripple of the buck boost and inverter stages. Although once again it cannot be made too small because of startup and other abnormal transient conditions. The required capacitance can be found from the buck boost converter current ripple ($\Delta I_1$), permitted voltage ripple ($\Delta V_2$), and on time ($\Delta T$).

$$C_2 = \frac{\Delta I_1 \Delta T}{\Delta V_2} \tag{2.9}$$

Similar to the buck boost inductance, the input capacitance has an effect on the eigenvalues of the plant for the input voltage control system. Figure 2.5 shows how increased capacitance results in reduced resonant frequency and lower bandwidth requirements.

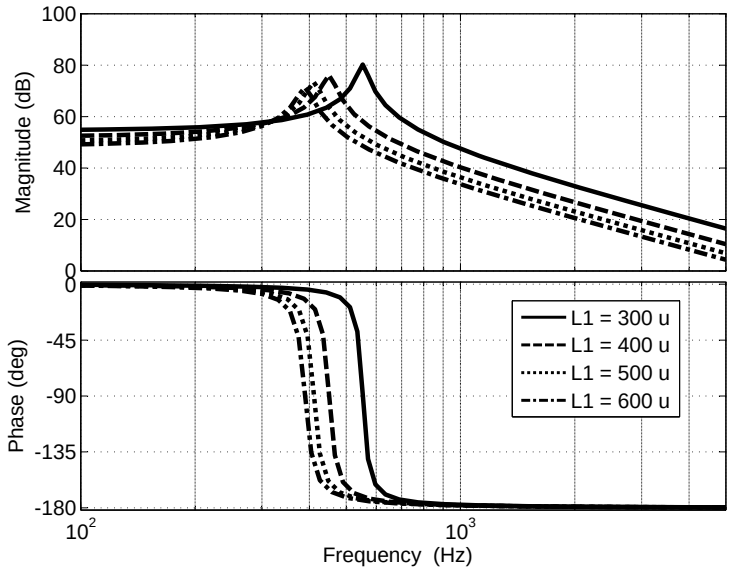


Figure 2.5: Frequency Response Variations with Change of Input Capacitance

## 2.4 Inverter Output Filter ($L_2$ and $L_3$)

One approach to select the inverter inductor is with maximum ripple current. This will be shown for the inductor associated with phase one. The average duty ratio of one half bridge (one phase leg) from Figure 2.1 is approximately a function of DC link capacitor voltages and instantaneous grid voltage ($v_5$).

$$d_2 \approx \frac{v_5 + V_1}{V_2 + V_1} \tag{2.10}$$

The required inductance is a function of instantaneous voltage across the inductor $(V_2 - v_5)$, duty ratio $(d_2)$, and permitted ripple $(\Delta I_2)$. The worst case condition occurs when the grid is at zero volts and the capacitors are at maximum voltage.

$$L_2 = \frac{(V_2 - v_5)d_2}{\Delta I_2 f_{sw}} \tag{2.11}$$

Inserting (2.10) into (2.11), and setting $v_5$ to zero, the required inductance is a function of ripple current.

$$L_2 = \left(\frac{V_2}{\Delta I_2 f_{sw}}\right)\left(\frac{V_1}{V_2 + V_1}\right) \tag{2.12}$$

With the maximum set to $10\ A$ at $550\ V$, the inductor peak-peak ripple current is shown below over half the fundamental period for several average voltages. Here both capacitor voltages are assumed to be equal.

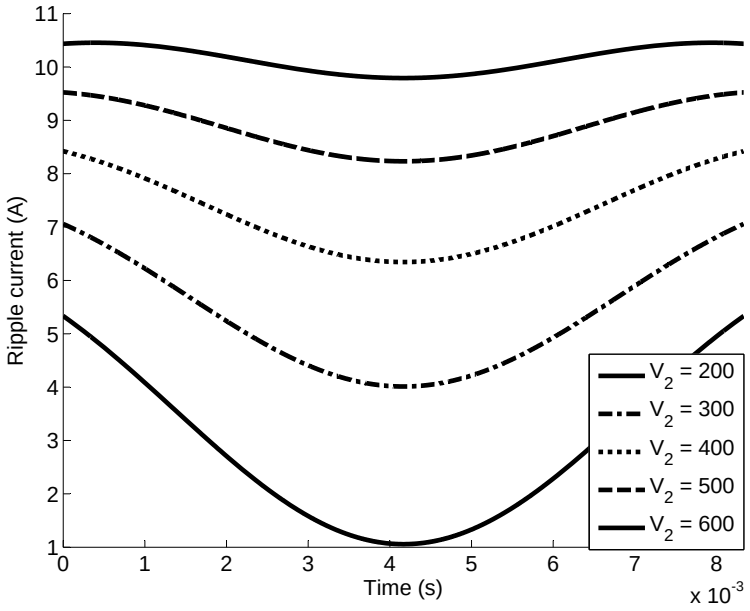


Figure 2.6: Time Varying Inverter Peak Ripple Current $(\Delta I_2)$ at Several Input Voltages

Chapter 3

# CONTROL SYSTEM

Control systems were developed for the buck boost converter and inverter circuits. The most important requirement is to maintain energy balance by regulating the average voltage across both capacitors. Also the converter should provide distortion free current to the grid. Before exploring the control systems for the circuit, a simple PV array model is presented because it should be considered for the input voltage control system.

## 3.1 Photovoltaic Array Model

A PV cell, panel, or array of panels can be modeled with sufficient accuracy with the circuit illustrated in Figure 3.1 [46] [47]. The current source $I_{ph}$ is the photon current at a particular temperature and irradiance (3.1). The diode current is given by equation (3.2). Parameters used in this study are listed in Table 3.1.

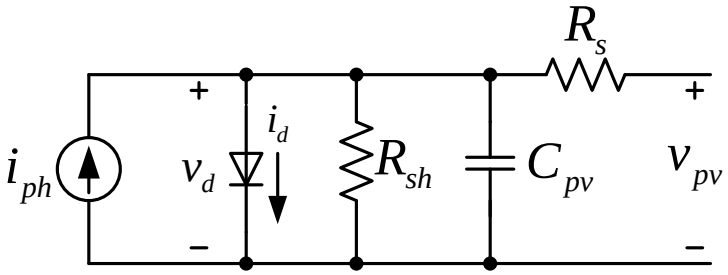


Figure 3.1: Equivalent Circuit of PV Panel

$$I_{ph} = (I_{sc} + K_I * \Delta T) * \frac{G}{G_{nom}} \tag{3.1}$$

$$I_d = I_o \left( e^{\frac{qV_d}{akTN_pN_s}} - 1 \right) \tag{3.2}$$

$$I_o = I_{o\_nom} \left( \frac{T_{nom}}{T} \right)^3 e^{\left( \frac{qEg}{akT} \left( \frac{1}{T_{nom}} - \frac{1}{T} \right) \right)} \tag{3.3}$$

$$I_{o\_nom} = \frac{I_{sc}}{e^{\left( \frac{.622q}{akT} - 1 \right)}} \tag{3.4}$$

This model was verified in simulation by sweeping the terminal voltage from short circuit to open circuit at nominal temperature. The performance plot is shown in Figure 3.3.

Table 3.1: Parameters for Photovoltaic Array Model

| DESCRIPTION | SYMBOL | VALUE |
|---|---|---|
| Number of cells in one panel | $N_s$ | $54$ |
| Number of panels | $N_p$ | $12$ |
| Short circuit current | $I_{sc}$ | $8.33\ A$ |
| Open circuit voltage | $V_{oc}$ | $33.6\ V$ |
| Nominal temperature | $T_{nom}$ | $298.15\ K$ |
| Temperature difference from nominal $(T - T_{nom})$ | $\Delta T$ | $K$ |
| Nominal irradiance | $G_{nom}$ | $1000\ W/m^2$ |
| Irradiance | $G$ | $W/m^2$ |
| Series resistance of array | $R_s$ | $.212 \times N_p\ \Omega$ |
| Shunt resistance of array | $R_{sh}$ | $400 \times N_p\ \Omega$ |
| Capacitance of array | $C_{pv}$ | $1e^{-8} \times N_p\ F$ |
| Temperature coefficient | $K_I$ | $.055e^{-2}$ |
| Electron charge | $q$ | $1.60218e^{-19}\ C$ |
| Material bandgap | $E_g$ | $1.12\ eV$ |
| Boltzman constant | $k$ | $1.38e^{-23}\ J/K$ |
| Ideality factor | $a$ | $1.2$ |

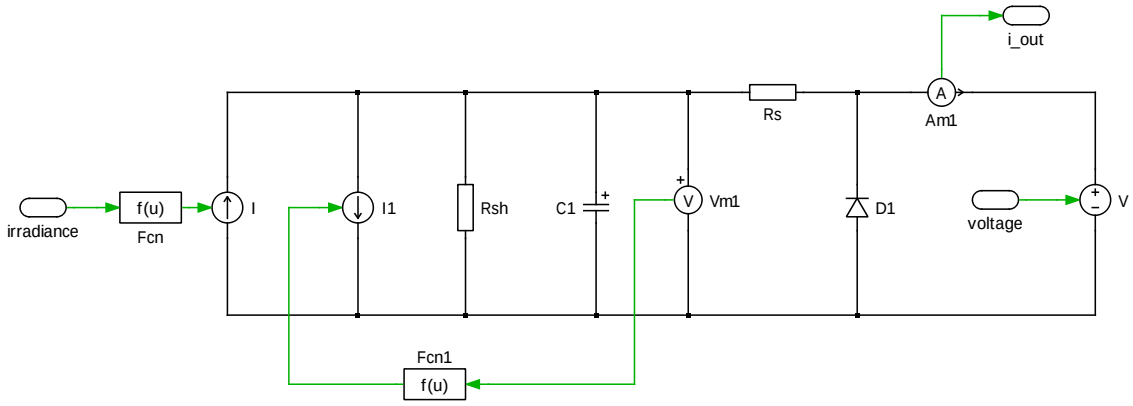


Figure 3.2: Simulation Diagram of PV Array

## 3.2 Buck Boost Control System

First a regulator was configured to clamp the input DC voltage ($v_2$) when subject to external currents. The complete buck boost converter closed loop control system is illustrated in Figure 3.4.

### 3.2.1 Buck Boost Plant

The bi-directional buck boost converter is illustrated in Figure 3.5 with the input PV current represented by $i_4$ and Norton resistance is $R_0$. Currents associated with the inverter stage are grouped together as low frequency disturbances $i_5$ and $i_6$. The circuit can be redrawn with average quantities (Figure 3.6) and as a state equation (3.5). The state vector is $x = \begin{bmatrix} v_1 & v_2 & i_1 \end{bmatrix}^T$, and the input vector

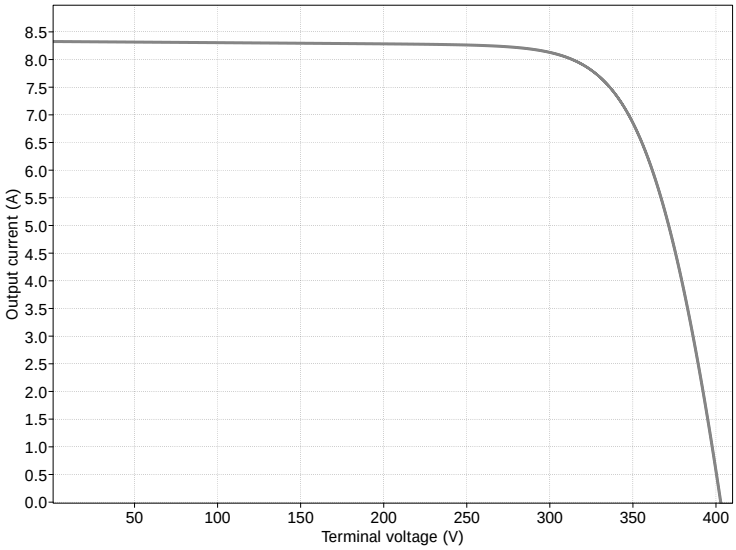


Figure 3.3: Simulation VI Plot of PV Array

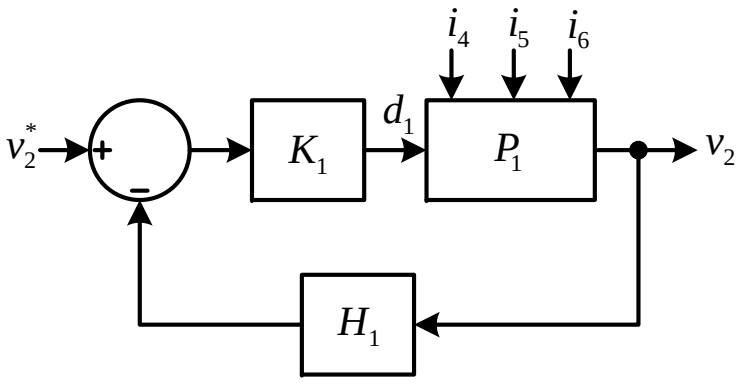


Figure 3.4: Buck Boost Control Loop

is $u = \begin{bmatrix} d_1 & i_4 & i_5 & i_6 \end{bmatrix}^T$.

$$f(x,u) = \begin{bmatrix} C_1 \dot{v_1} \\ C_2 \dot{v_2} \\ L_1 \dot{i_1} \end{bmatrix} = \begin{bmatrix} -i_1 + d_1 i_1 + i_6 \\ i_4 + d_1 i_1 - i_5 - v_2/R_0 \\ -d_1 v_2 - i_1 R_1 + v_1 - d_1 v_1 \end{bmatrix} \tag{3.5}$$

The average model was validated in simulation under open loop conditions while subjected to various input steps. Figure 3.7 shows the state variables of the average model compared with the switching model while subject to a duty ratio step at 2.5 seconds. The dashed trace is the average model.

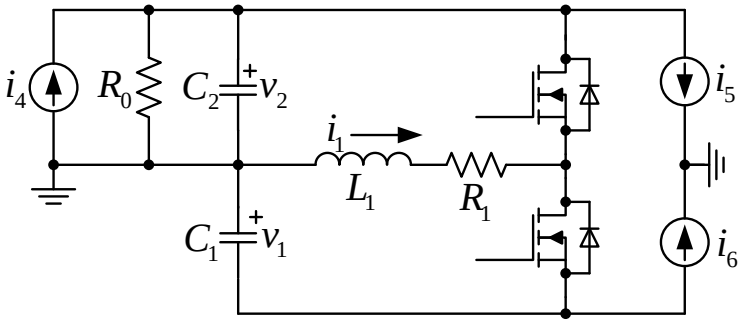


Figure 3.5: Switching Model of Buck Boost Converter

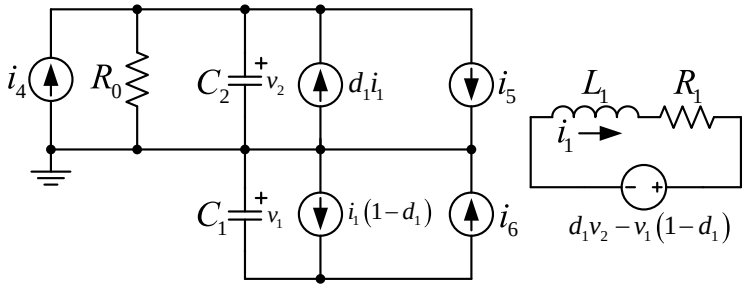


Figure 3.6: Average Model of Buck Boost Converter

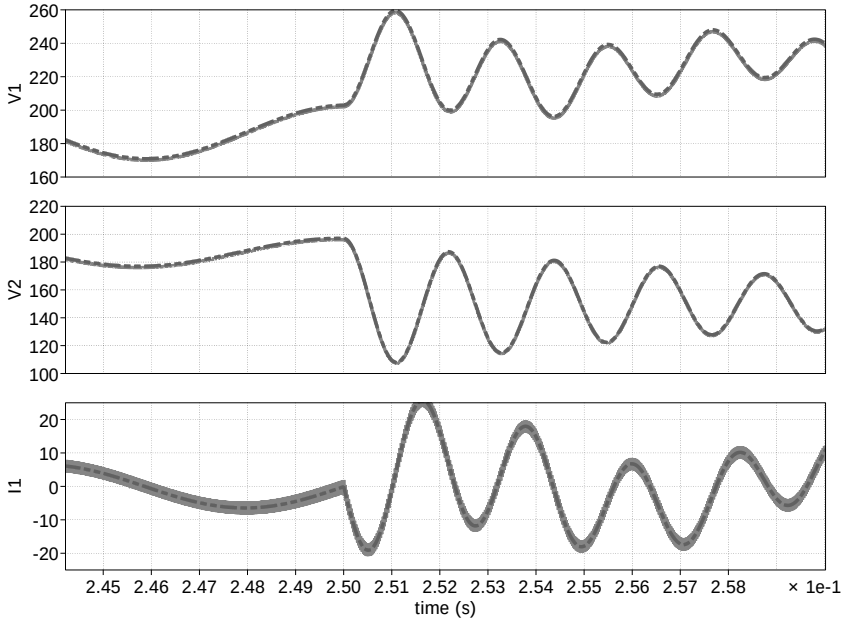


Figure 3.7: Buck Boost Average Plant Validated Against Switching Model

Linearization of (3.5) results in a state space model (3.8) for control design.

$$A_p = Y^{-1}\frac{\partial f}{\partial x}\Big|_{(x_e,u_e)} \tag{3.6}$$

$$B_p = Y^{-1}\frac{\partial f}{\partial u}\Big|_{(x_e,u_e)} \tag{3.7}$$

$$\begin{aligned} A_p &= Y^{-1}\begin{bmatrix} 0 & 0 & (d_1-1) \\ 0 & -1/R_0 & d_1 \\ (1-d_1) & -d_1 & -R_1 \end{bmatrix}_{(x_e,u_e)} \qquad B_p = Y^{-1}\begin{bmatrix} i_1 & 0 & 0 & 1 \\ i_1 & 1 & -1 & 0 \\ -(v_1+v_2) & 0 & 0 & 0 \end{bmatrix}_{(x_e,u_e)} \\ C_p &= \begin{bmatrix} 0 & -1 & 0 \end{bmatrix} \; D_p = \begin{bmatrix} 0 \end{bmatrix} \end{aligned} \tag{3.8}$$

Where $Y = diag\,(C_1 \;\; C_2 \;\; L_1)$. The $C$ matrix is shown negated such that a positive relationship exists between $d_1$ and $v_2$. The linear plant can also be written with the B matrix decomposed such that disturbances may be evaluated separately.

$$\dot{x} = A_p x + B_{p1} d_1 + B_{p2} i_4 + B_{p3} i_5 + B_{p4} i_6 \tag{3.9}$$

Where

$$A_p = \begin{bmatrix} 0 & 0 & (1/C_1)(d_1-1) \\ 0 & -1/(C_2R_0) & d_1/C_2 \\ (1/L_1)(1-d_1) & -d_1/L_1 & -R_1/L_1 \end{bmatrix}_{(x_e,u_e)} \tag{3.10}$$

$$B_{p1} = \begin{bmatrix} i_1/C_1 \\ i_1/C_2 \\ -(v_1+v_2)/L_1 \end{bmatrix}_{(x_e,u_e)} \tag{3.11}$$

$$B_{p2} = \begin{bmatrix} 0 \\ 1/C_2 \\ 0 \end{bmatrix} \tag{3.12}$$

$$B_{p3} = \begin{bmatrix} 0 \\ -1/C_2 \\ 0 \end{bmatrix} \tag{3.13}$$

$$B_{p4} = \begin{bmatrix} 1/C_1 \\ 0 \\ 0 \end{bmatrix} \tag{3.14}$$

Equilibrium solutions were found with Maple computer algebra software. The linear plant was then evaluated at the equilibrium points. The worst case phase lag was found to occur at zero PV current. Figure 3.8 shows the buck boost converter plant frequency response (duty to input voltage) at several equilibrium conditions.

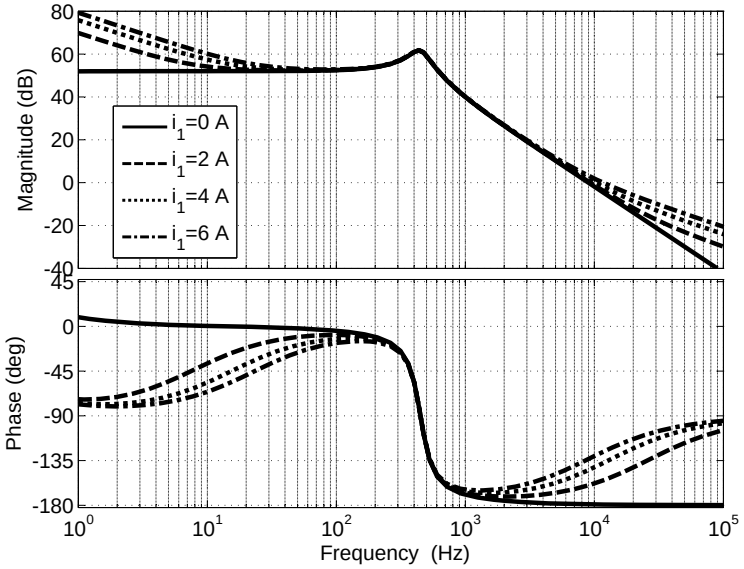


Figure 3.8: Buck Boost Frequency Response (from $d_1$ to $v_2$)

The plant was also evaluated at several source impedances as in [47] to investigate its effect on the plant and system stability. According to the maximum power transfer theorem, the maximum power point occurs when the source impedance is equal to the inverter impedance $Z_{inv} = Z_{pv}^*$. Neglecting PV capacitance, this occurs when the source resistance $(R_0)$ is equal to the inverter incremental impedance $(v_{in}/i_{in})$. PV capacitance is not included in the small signal model because the input capacitance $C_2$ is much larger, and in parallel with the array capacitance. Figure 3.9 shows the bode diagram of the buck boost plant with the PV array impedances below, at, and above the maximum power point at a specific operating condition. Various array conditions have an effect only on low frequency behavior.

### 3.2.2 Buck Boost Control Synthesis

The control system was designed with consideration of both reference and disturbance inputs. A third order lag lead controller as in [48] was set with 600 Hz crossover. An internal model resonant term as in [49] was included such that double line frequency disturbance currents are attenuated.

$$K_1(s) = \frac{K_i(s/\omega_z + 1)^2}{s(s/\omega_p + 1)^2} + \frac{K_r s}{s^2 + \omega_r^2} \tag{3.15}$$

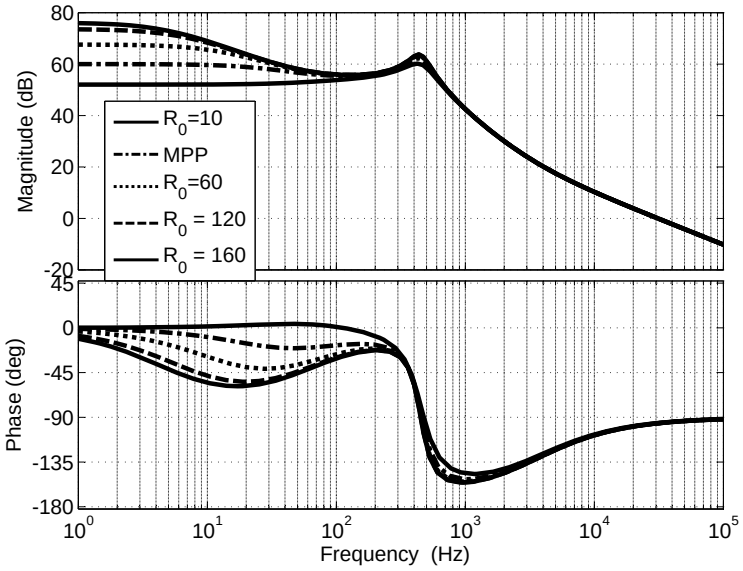


Figure 3.9: Small Signal Frequency Response with Various Array Impedances

The open loop frequency response of (3.16), illustrated in Figure 3.10, shows the desired crossover frequency with $60^\circ$ phase margin and infinite gain at DC and 120 Hz. This plot also illustrates how the bandwidth varies with parametric variations of the inductance.

$$Loop_1(s) = H_1 P_1 K_1 \tag{3.16}$$

The loop gain was also measured in closed loop operation with the Plexim PLECS loop gain analysis simulation tool. The average non-linear equation model was implemented for the plant along with the nominal linear controller. Figure 3.11 shows the response measured in simulation closely matches the predicted model. The 120 Hz resonance is apparent and the desired crossover is correct.

The loop response was also verified in hardware. An AP Instruments 102B network analyzer was arranged to perturb the loop in closed loop operation. Figure 3.12 shows how the frequency sweep signal is injected into the loop along with input/output measurement points. The resultant transfer function is the negated open loop response (3.17).

$$\frac{v_o}{v_i} = -H_1 P_1 K_1 = -Loop_1 \tag{3.17}$$

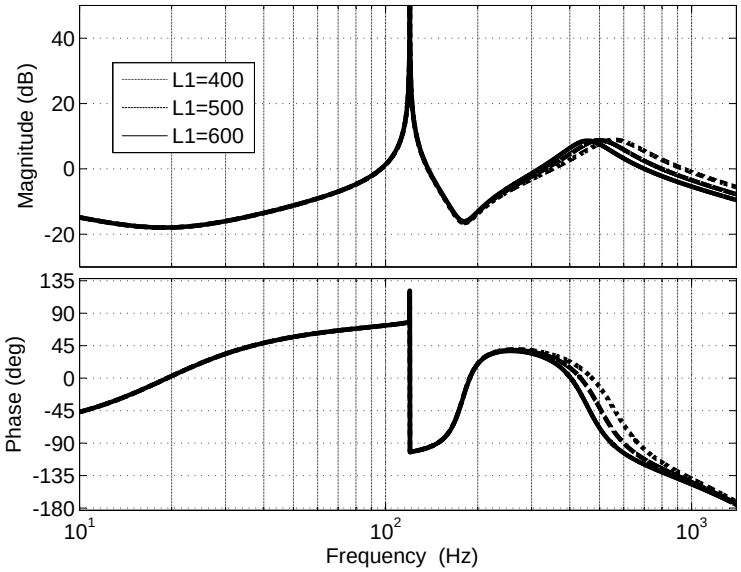


Figure 3.10: Buck Boost Converter Open Loop Response with Variations in Inductance

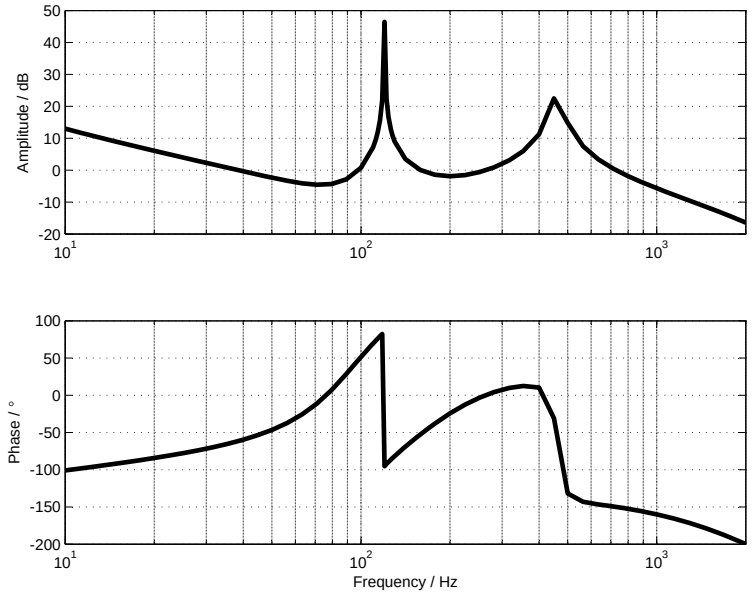


Figure 3.11: Loop Response Measured with PLECS Loop Gain Analysis Block

The closed loop system is then evaluated for robustness with parametric variations of the inductance. As shown in the chapter discussing design of the inductor, the permeability and in turn inductance, changes with load conditions. The closed loop system associated with reference and disturbances (3.18) and (3.19) are derived from the expanded control loop diagram of Figure 3.14. Figures 3.15 - 3.19 show

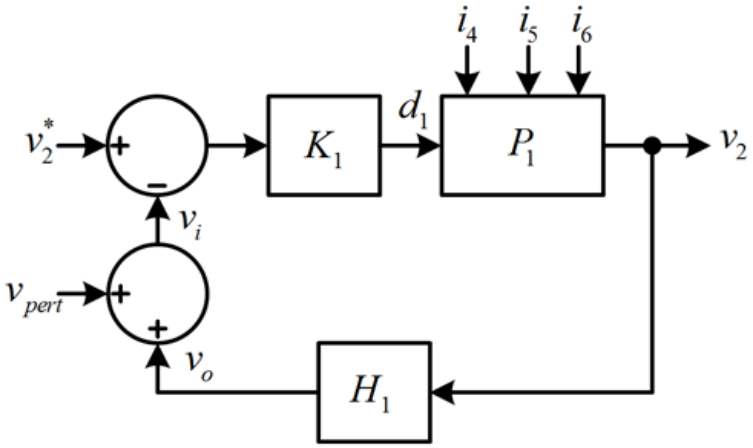


Figure 3.12: Loop Response Measurement Setup

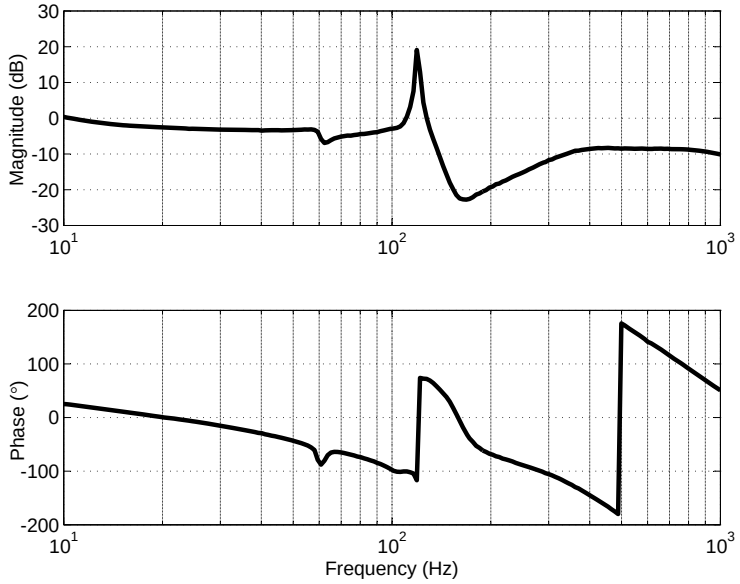


Figure 3.13: Measured Open Loop Response

how the closed loop system is affected by variations of inductance.

$$\begin{bmatrix} \dot{x_p} \\ \dot{x_k} \\ \dot{x_f} \end{bmatrix} = \begin{bmatrix} A_p & B_{p1}C_k & 0 \\ 0 & A_k & -B_kC_f \\ B_fC_p & 0 & A_f \end{bmatrix} \begin{bmatrix} x_p \\ x_k \\ x_f \end{bmatrix} + \begin{bmatrix} 0 \\ B_k \\ 0 \end{bmatrix} r + \begin{bmatrix} B_{p2} \\ 0 \\ 0 \end{bmatrix} i_4 + \begin{bmatrix} B_{p3} \\ 0 \\ 0 \end{bmatrix} i_5 + \begin{bmatrix} B_{p4} \\ 0 \\ 0 \end{bmatrix} i_6 + \begin{bmatrix} 0 \\ 0 \\ B_f \end{bmatrix} n \tag{3.18}$$

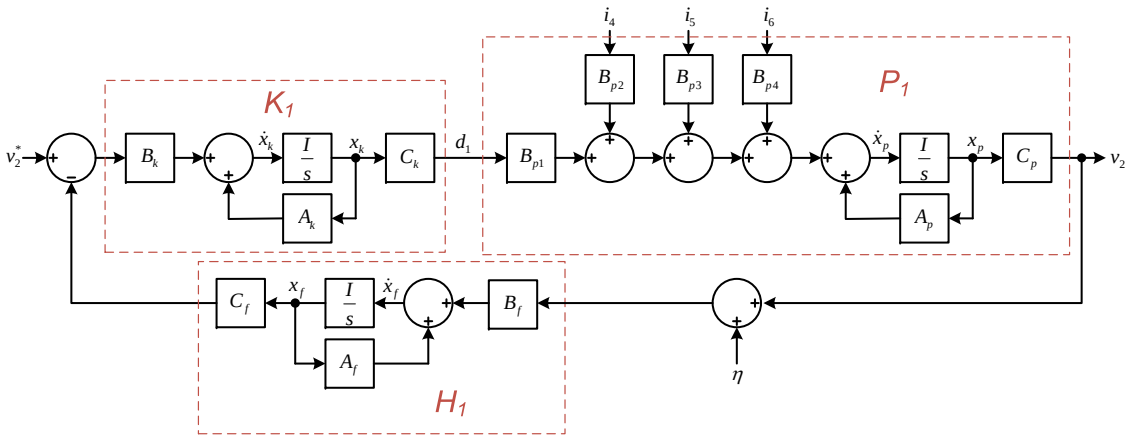


Figure 3.14: Buck Boost Control Loop with Disturbance Details

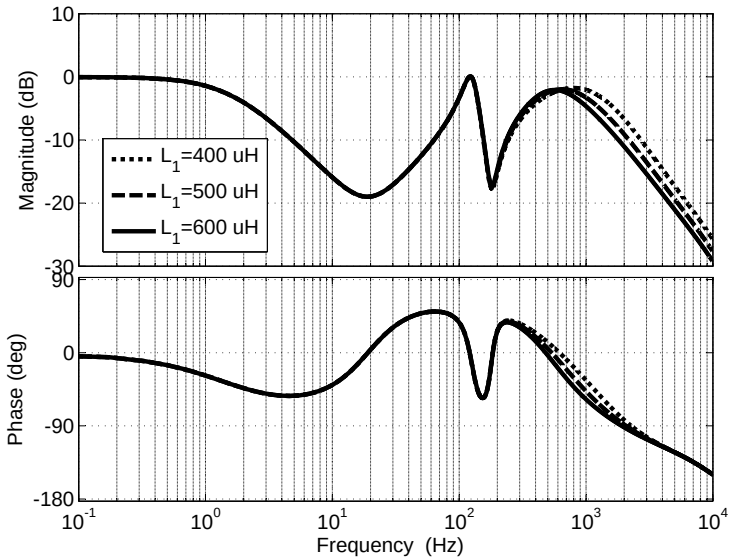


Figure 3.15: Closed Loop Tracking of Reference While Subject to Changes in Inductance

$$y = \begin{bmatrix} C_p & 0 & 0 \end{bmatrix} \begin{bmatrix} x_p \\ x_k \\ x_f \end{bmatrix} \tag{3.19}$$

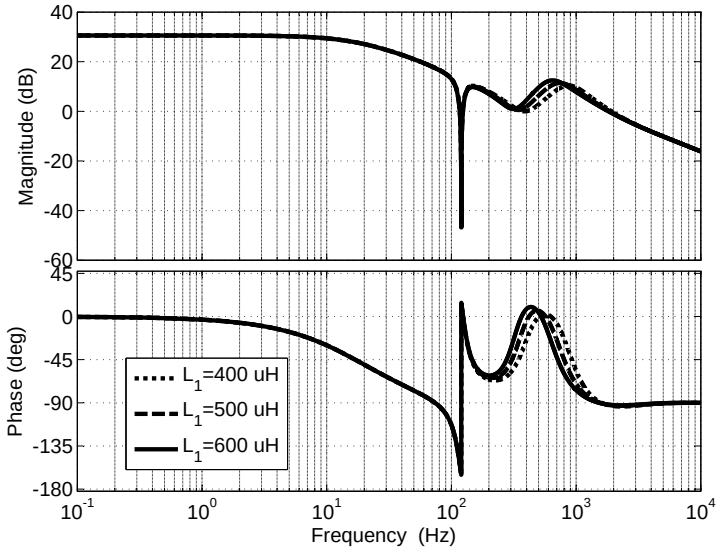


Figure 3.16: Closed Loop Attenuation of Inverter Disturbance Current $i_5$

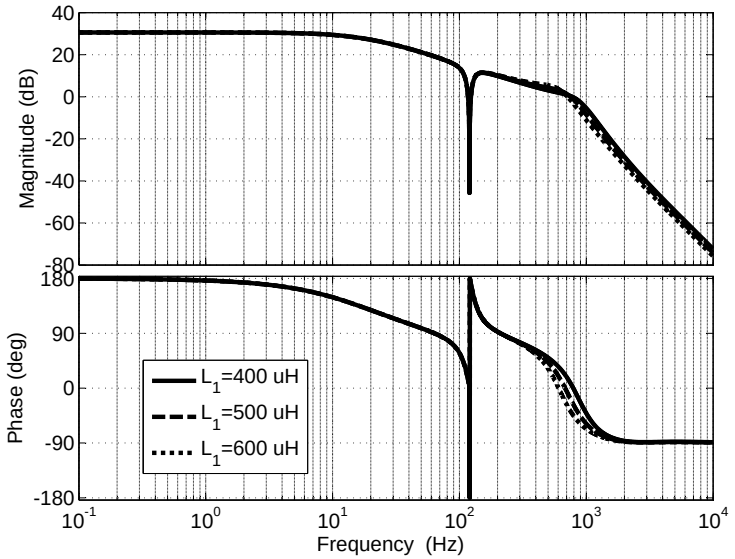


Figure 3.17: Closed Loop Attenuation of Inverter Disturbance Current $i_6$

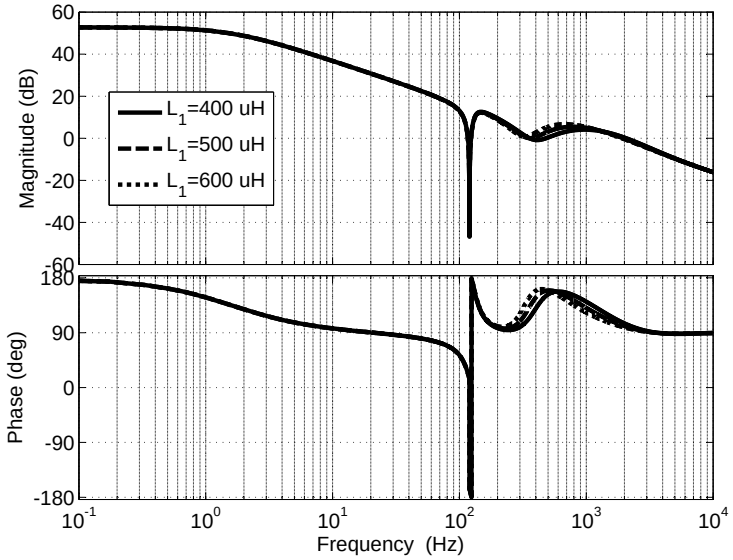


Figure 3.18: Closed Loop Attenuation of Input Current Disturbance

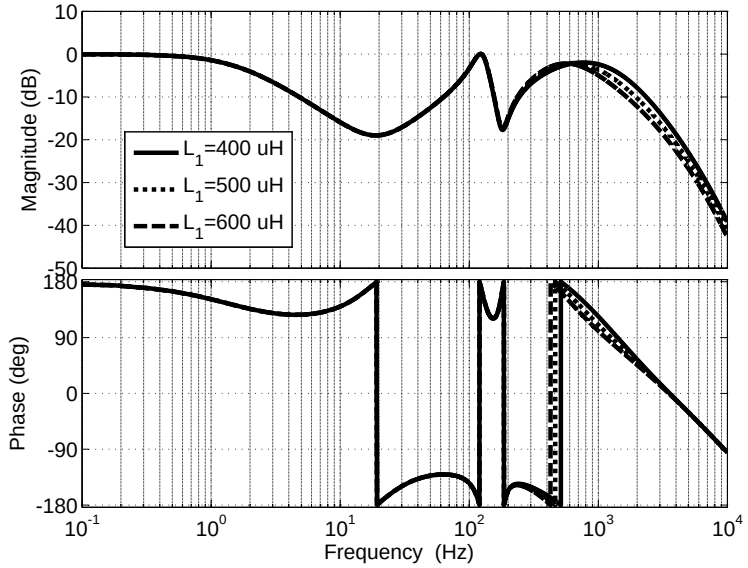


Figure 3.19: Closed Loop Attenuation of Noise

## 3.3 Inverter Control System

As depicted in Figure 3.20, the inverter control system is comprised of a cascaded loop for regulating the average voltage across the bottom side capacitor $(C_1)$ and the grid current wave shape.

### 3.3.1 Energy Balance Controller

An energy balance controller $(K_3)$ was developed to regulate the average value of $v_1$ through the grid current magnitude reference of both phase legs.

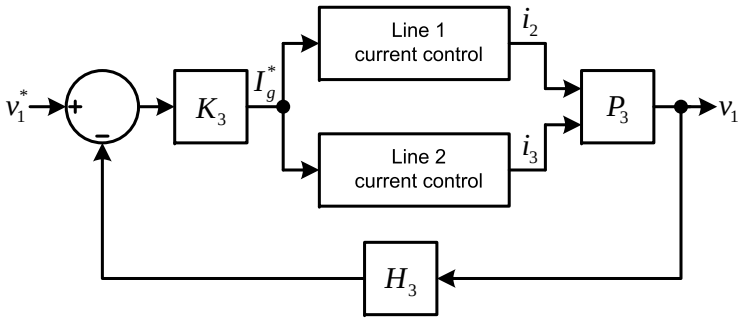


Figure 3.20: Energy Balance Control Loop

Power balance is applied to determine an appropriate plant. Power absorbed by the grid is as follows where $\phi$ is the phase angle displacement between voltage and current.

$$p_g(t) = \frac{V_g I_g \cos(\phi)}{2} + \frac{V_g I_g \cos(2\omega t + \phi)}{2} \tag{3.20}$$

Also capacitor power is the first derivative of capacitor energy.

$$p_{C_1}(t) = \frac{d}{dt}\left(\frac{1}{2} C_1 v_1^2(t)\right) \tag{3.21}$$

A transfer function may then be created from (3.20) and (3.21).

$$P_3(s) = \frac{v_1^2}{I_g} = -\frac{V_g}{sC_1} \tag{3.22}$$

The plant is linear when regulating the squared capacitor voltage. A second order lag/lead regulator (3.23) was set with a 20 Hz bandwidth for this outer loop. Open loop response of (3.24) is illustrated in Figure 3.21.

$$K_3(s) = \frac{K(s/\omega_z + 1)}{s(s/\omega_p + 1)} \tag{3.23}$$

$$Loop_3(s) = H_3 P_3 K_3 \tag{3.24}$$

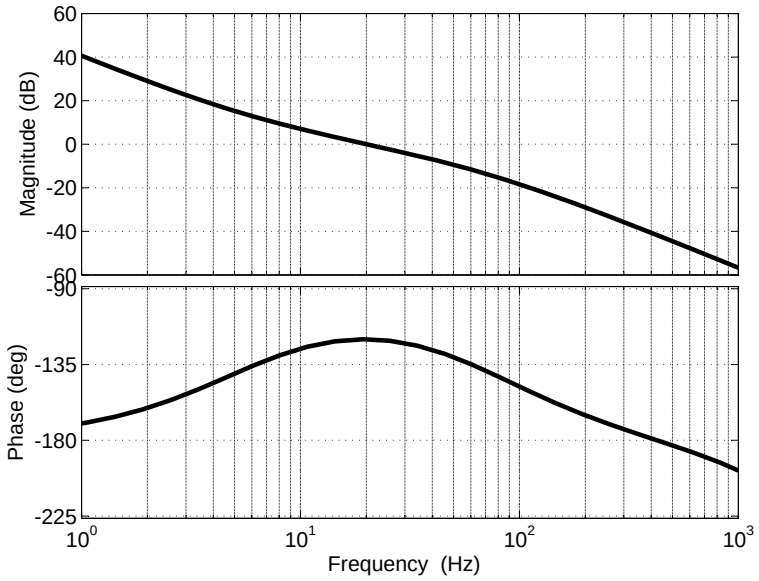


Figure 3.21: Energy Balance Control System Open Loop Response

The open loop response was validated in simulation. The simulation validation entailed running the circuit in closed loop with average models of the switching circuit. The grid current, (inner loop) controllers were active. The input was approximated with a voltage source. A perturbation signal was injected into the loop in a similar manner as in Figure 3.12. Results of the simulation show most importantly the desired crossover is correct. Although there is some influence from the current controllers that is evident.

The loop response was also evaluated in hardware. Figure 3.23 shows results from experiment. The crossover is slightly below what is predicted. Frequencies below 10 Hz were not attainable with the experiment because of AC coupling requirements.

### 3.3.2 Grid Current Plant

At small time scales the inverter can be approximated with constant DC link voltages. The average model of the switching circuit (Figure 3.24) is shown in Figure 3.25.

The half bridge inverter plants are decoupled and simplified as first order systems.

$$P_2(s) = \frac{i_2}{v_x} = \frac{1}{sL_2 + R_2} \tag{3.25}$$

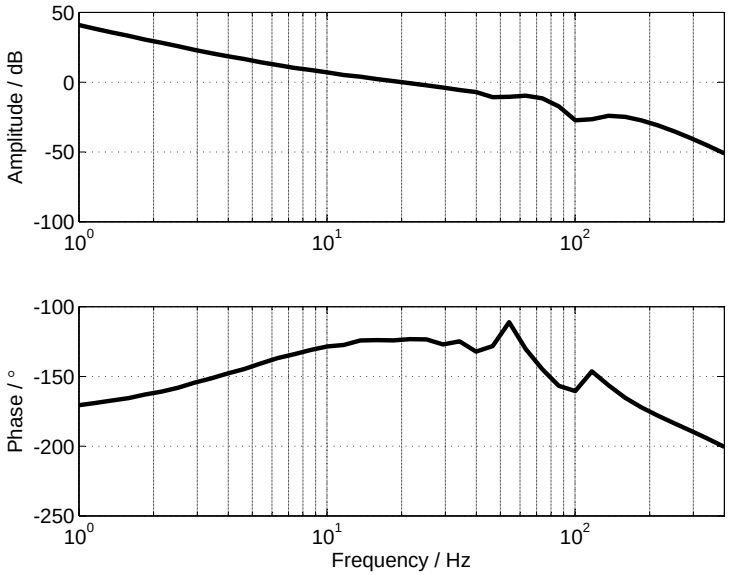


Figure 3.22: Energy Balance Control System Open Loop Response from Simulation

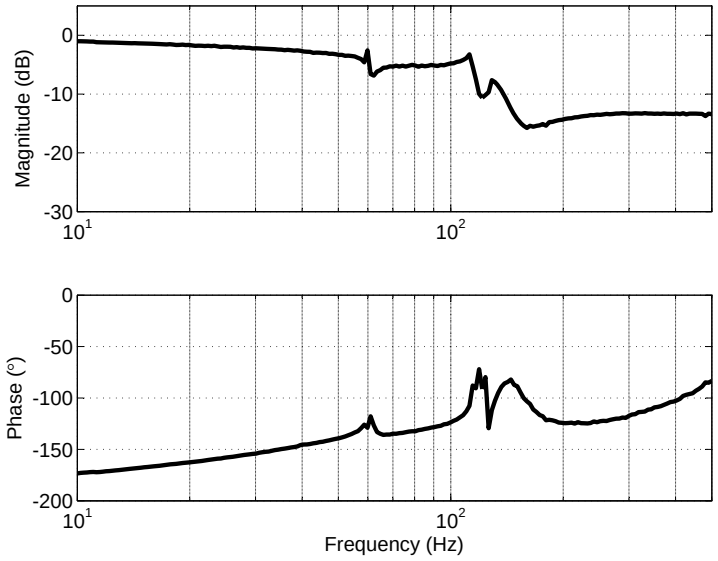


Figure 3.23: Energy Balance Control System Open Loop Response from Experiment

### 3.3.3 Grid Current Control Synthesis

Each phase has separate anti-alias filters, Phase Locked Loops (PLL), and current controllers as shown in Figure 3.26. The PLL provides a sinusoidal wave shape synchronized with the grid; the magnitude reference is from the outer energy balance loop.

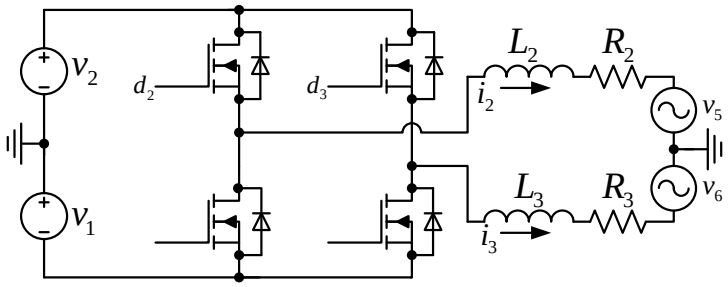


Figure 3.24: Split Phase Inverter Switching Model

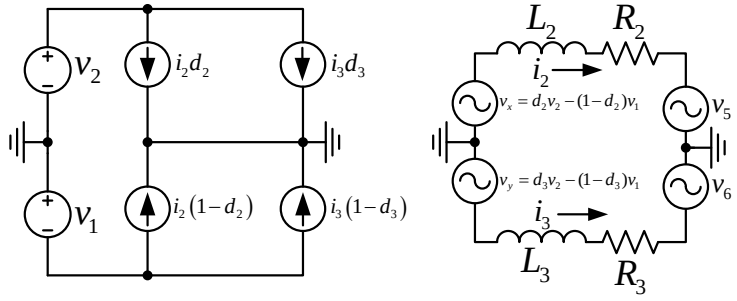


Figure 3.25: Inverter Average Model

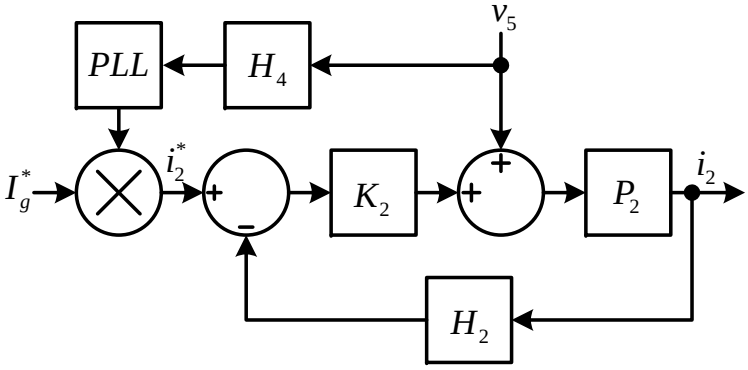


Figure 3.26: Inner Current Control Loop of One Phase Leg

The average voltage at the power pole ($v_x$), as shown in Figure 2.1, can be influenced by variations from each of the capacitor voltages. Linear control design is possible when the average inverter voltage $(v_x)$ is precisely synthesized. A modulating function is thus utilized to calculate the duty from controller output $(v_x^*)$ and instantaneous measured capacitor voltages. This essentially rejects disturbances associated with the capacitor voltages.

$$v_x = d_2 v_2 - (1 - d_2)v_1 \Rightarrow d_2 = \frac{v_x + v_1}{v_2 + v_1} \tag{3.26}$$

A proportional resonant controller [49] with grid voltage feed forward was found to work well with a 400 Hz bandwidth. Although the feed forward can be prone to injecting noise into the loop, it is important to include this such that starts up transients are not an issue.

$$K_2(s) = K_p + \frac{K_i s}{s^2 + \omega_0^2} \tag{3.27}$$

$$Loop_2(s) = H_2 P_2 K_2 \tag{3.28}$$

The current control open loop response (3.28) is shown in Figure 3.27. Once again the open loop response was validated in simulation and with hardware. The simulation results of Figure 3.28 shows a phase margin greater than predicted. Hardware results indicate the loop is approximately modeled correctly.

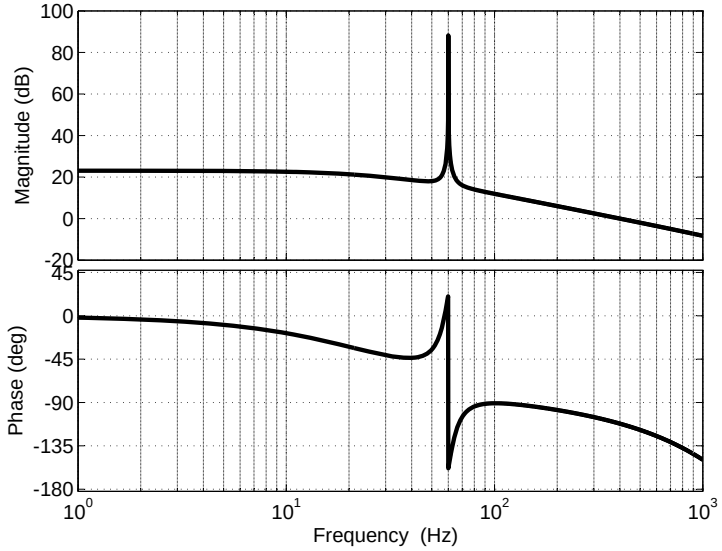


Figure 3.27: Inverter Open Loop Response

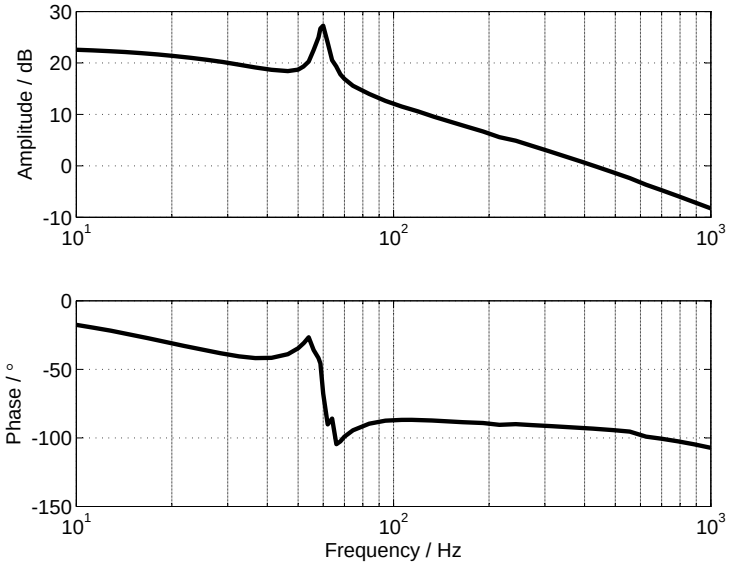


Figure 3.28: Inverter Open Loop Response Simulated

# Chapter 4

# EFFICIENCY

An analytic efficiency approximation is presented here. This is a non-trivial task that includes various aspects of electrical engineering. This study includes power dissipated in the semiconductor and magnetic elements. First the power semiconductor losses are evaluated. Switching transition energies are found with several different approaches. Semiconductor conduction losses are also considered. Results of the semiconductor study are then used to predict junction temperatures of the power switches. The inductor core and wire losses inductors are also evaluated. Semiconductor and inductor losses are then combined to show how the proposed converter might perform.

## 4.1 Semiconductor Transition Energy From Data Sheet

The power semiconductors to be utilized in the study are silicon carbide (SiC), N-channel, enhancement mode MOSFETs manufactured by Cree Semiconductor. Some of the data sheet parameters and symbols are repeated in Table 4.1.

Important information that is necessary to find an analytic solution of switching losses is the transition energy as a function of current. These plots are provided in the device data sheet at a fixed $800\ V$ drain-source voltage. A polynomial fit was applied to the data to attain an equation for both turn on and turn off transition energy as a function of current. Alternatively, as presented later, these plots may also be created from circuit parameters and operating conditions or from direct measurements.

The turn on and turn off equations of Figures 4.1 and 4.2 can be combined into a second order polynomial that gives the total energy dissipated per switching cycle. This will be used later to determine

Table 4.1: Parameters for Cree CMF10120D

| **DESCRIPTION** | **SYMBOL** | **VALUE** |
|---|---|---|
| On state resistance | $R_{ds}$ | $160\ m\Omega$ |
| Gate plateau voltage | $V_{plat}$ | $10\ V$ |
| Gate to source charge | $Q_{gs}$ | $11.8\ nC$ |
| Gate to drain charge | $Q_{gd}$ | $21.5\ nC$ |
| Reverse recovery charge of body diode | $Q_r$ | $94\ nC$ |
| Total gate charge | $Q_g$ | $47.1\ nC$ |
| Internal gate resistance | $R_g$ | $13.6\ \Omega$ |
| Current rise time | $t_{ri}$ | $14\ ns$ |
| Current fall time | $t_{fi}$ | $37\ ns$ |

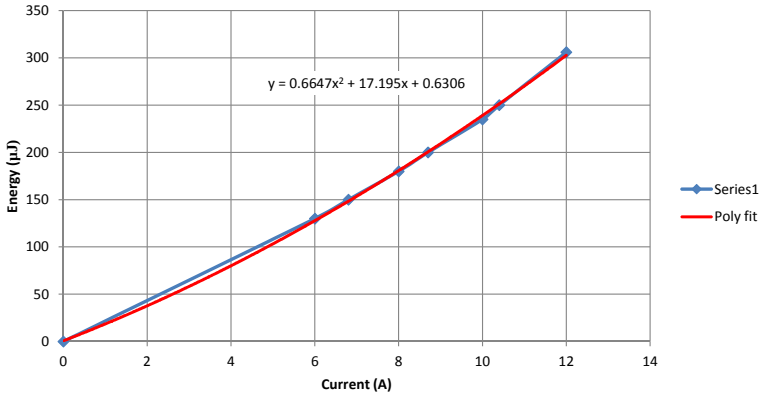


Figure 4.1: Turn On Transition Energy for Cree CMF10120D

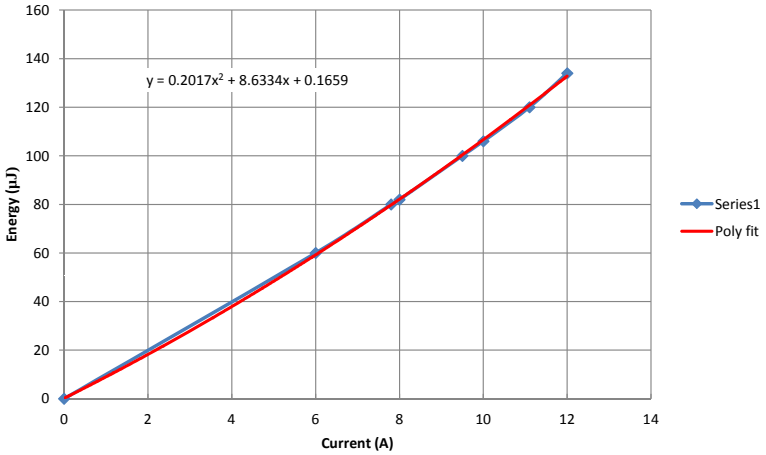


Figure 4.2: Turn Off Transition Energy for Cree CMF10120D

Table 4.2: Parameters for Cree C4D10120A

| DESCRIPTION | SYMBOL | VALUE |
|---|---|---|
| Nominal on-state voltage drop | $V_f$ | $1.5\,V$ |
| Reverse recovery charge | $Q_c$ | $66e^{-9}\,C$ |

the average power dissipated.

$$E_{tot} = E_{on} + E_{off} = ai^2 + bi + c \tag{4.1}$$

As suggested in [50], a SiC Schottky Barrier Diode (SBD) should be included to bypass the low performance body diode of the MOSFET. Some of the data sheet parameters for such a diode are repeated in Table 4.2.

## 4.2 Alternative Approach to Determine Switching Transition Energy

If the transition energy plots are not provided, or if it is desirable to utilize an arbitrary current and voltage, approximation techniques have been developed [51]. This approach mostly entails identifying transition times.

When a transition occurs, voltage and current overlap results in power dissipated within the transistor. The plot of instantaneous power is approximately triangular with the peak of the triangle the product of instantaneous current and voltage. At turn on transition, the triangle base is the sum of current rise $(t_{ri})$ and voltage fall $(t_{vf})$ times. The area of the triangle is the energy dissipated (4.2). This transition energy equation is an alternative to the polynomial expression of (4.1).


Figure 4.3: Approximation of Instantaneous Switching Power

$$E_{on} = \frac{VI(t_{ri} + t_{fv})}{2} \tag{4.2}$$

To find these transition times it is necessary to look at dynamics of the transistor. Switching MOSFET characteristics are mostly dictated by the device capacitances of Figure 4.4 [52].

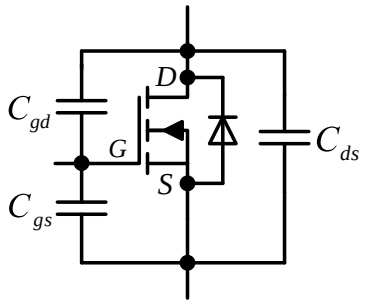


Figure 4.4: Parasitic Capacitances of Power MOSFET

A brief description of the switching process is explained in context of a turn on event. As the gate voltage increases, current flows into the gate capacitances $C_{gd}$ and $C_{gs}$. Once the gate threshold

voltage has been reached, drain to source current begins to increase. When the gate voltage reaches the plateau level, the gate current is mostly feeding the Miller $(C_{gd})$ capacitor; the voltage across the device begins to fall at this point. Also the output capacitance $(C_{ds})$ is discharged during the voltage fall interval. Once the switch is fully on, the gate voltage begins to increase again to its final value. The sequence is depicted in Figure 4.5 in terms of stored charge [53]. The current rise time is associated with $Q_{gs2}$ and the voltage fall time is associated with $Q_{gd}$.

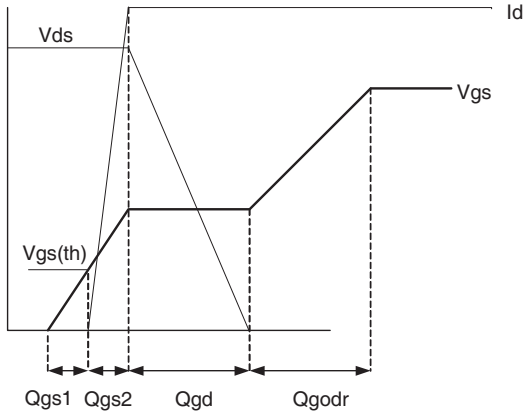


Figure 4.5: MOSFET Turn On Behavior

The current rise time is often provided in the data sheet as $t_{ri}$. The rise time could also be measured. Or, if available, the rise time can be found as a change in charge $Q_{gs2}$ after the threshold has been reached until the plateau region (4.3). This charge is however not always provided in the data sheet.

$$t_{ri} = \frac{Q_{gs2}}{I_{gate}} \tag{4.3}$$

The gate current $I_{gate}$ is found from the driver voltage, gate resistor, and plateau voltage.

$$I_{gate} = \frac{V_{drive} - V_{plat}}{R_g} \tag{4.4}$$

The voltage fall time $(t_{fv})$ can be approximated from the gate current, Miller capacitance, and drain-source voltage change (4.5). A slightly more detailed version that includes voltage dependent capacitance is described in [51]. Or the fall time can be found from a change in Miller charge as a result of the gate current (4.6).

$$t_{vf} = (V_{Q3\_on})\frac{C_{gd}}{I_{gate}} \tag{4.5}$$

$$t_{vf} = \frac{Q_{gd}}{I_{gate}} \tag{4.6}$$

Once the transition times are known, the transition energy can be found from the triangular approximation (4.2). Turn off transitions are similar with the exception that the drain to source capacitor charge is not dissipated at turn off.

## 4.3 Buck Boost Semiconductor Losses

Power dissipated in switching transistors are mostly associated with switching and conduction losses.

First a few equations for the bi-directional buck boost converter of Figure 4.6 are listed. These are needed to determine various steady state (large signal) circuit parameters for the semiconductor study. The input current is $I_{in}$, and in steady state, the load current is the same as output current $I_{out}$.

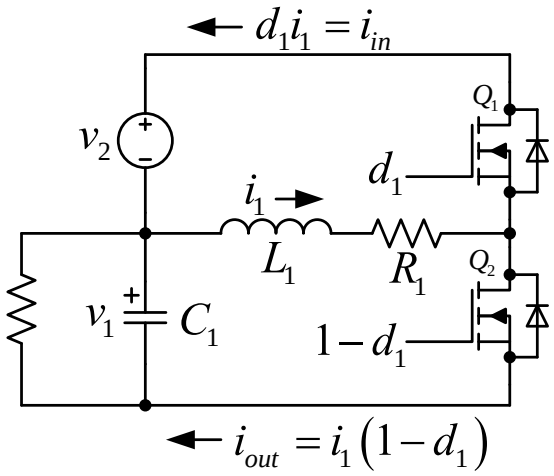


Figure 4.6: Basic Bi-directional Buck Boost Converter

The voltages, currents, and average inductor current are related in a large signal (DC) sense to the input average duty ratio signal $D_1$.

$$\frac{V_1}{V_2} = \frac{D_1}{1 - D_1} \Rightarrow D_1 = \frac{V_1}{V_1 + V_2} \tag{4.7}$$

$$\frac{I_{out}}{I_{in}} = \frac{1 - D_1}{D_1} \tag{4.8}$$

$$I_1 = \frac{I_{in}}{D_1} \tag{4.9}$$

Where $D_1 \in [0, 1]$

Furthermore, as discussed in Chapter 2, the inductor current ripple (peak-peak magnitude) is a function of duty ratio, switching frequency, inductance, and input voltage.

$$\Delta I_1 = \left(\frac{V_2}{L_1}\right)\left(\frac{D_1}{f_{sw}}\right) \tag{4.10}$$

The inductor average and ripple current are later used to determine voltages and currents across the semiconductor at various switching transition instants.

### 4.3.1 Buck Boost Conduction Losses

The average conduction loss over the switching cycle is found by averaging the instantaneous power dissipated in each transistor over a switching cycle [51]. The solution of the integral includes the transistor's RMS current.

$$P_{Q1\_cond} = \frac{1}{T_{sw}}\int_0^{T_{sw}} R_{ds} i_{Q1}^2(\tau)d\tau = R_{ds} I_{Q1\_rms}^2 \tag{4.11}$$

When the inductance is sufficiently large, the current waveform approximates a square wave. The RMS current of a square wave is a function of the magnitude and duty.

$$I_{Q1\_rms} = I_1\sqrt{D_1} \tag{4.12}$$

The duty ratio is different for the bottom side transistor $(Q_2)$.

$$I_{Q2\_rms} = I_1\sqrt{1 - D_1} \tag{4.13}$$

Once the RMS current is known, the conduction power dissipated can be found from (4.11). However the on state resistance is not exactly constant over operating temperatures. If the datasheet provides sufficient information, a method discussed in [51] may be applied to approximate the on state resistance as a function of junction temperature.

$$R_{ds}(T_j) = R_{ds}(25°C)\left(1 + \frac{k}{100}\right)^{T_j - 25°C} \tag{4.14}$$

### 4.3.2 Buck Boost Switching States

Before investigating switching losses for the bi-directional buck boost converter, it is necessary to identify the three different operating modes. The direction of current through the inductor at transition instant differentiates the modes.

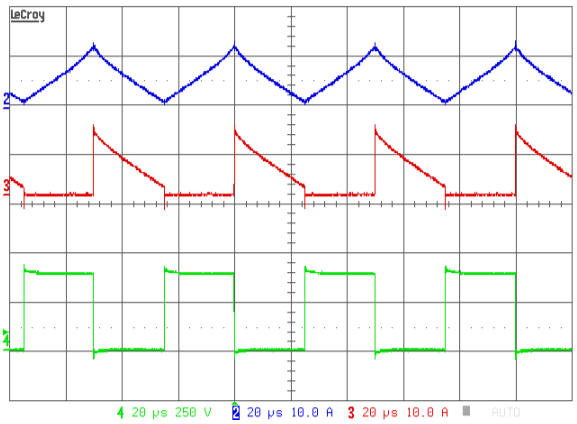


Figure 4.7: Experiment Results of Inductor Current (trace 2), $Q_2$ Current (trace 3), and $Q_2$ Voltage (trace 4) with Positive Current Transitions

The first case to consider is when the inductor current is positive at both transitions. Inductor current experiment results are shown in Figure 4.7, and the corresponding switching sequence is illustrated in Figure 4.8.

The bottom switch $(Q_2)$ always experiences hard switched transitions (non-zero current and voltage at switching instant). The top switch $(Q_1)$ always experiences Zero Voltage Switching (ZVS) because of the anti-parallel diode is conducting before and after switching events.

Switch and diode currents at instant of transition are given by (4.15) and (4.16). The transition voltage (when applicable) is always the sum of both capacitor voltages.

$$I_{Q_{1\_on}} = I_{Q_{2\_off}} = I_1 - \frac{\Delta I_1}{2} \tag{4.15}$$

$$I_{Q_{1\_off}} = I_{Q_{2\_on}} = I_1 + \frac{\Delta I_1}{2} \tag{4.16}$$

$$V_{Q_{1\_on}} = V_{Q_{1\_off}} \approx 0 \tag{4.17}$$

$$V_{Q_{2\_on}} = V_{Q_{2\_off}} = V_1 + V_2 \tag{4.18}$$

In the next case, the instantaneous inductor current changes direction; $Q_1$ switches on at negative current and $Q_2$ switches on at positive current. This is depicted in Figure 4.9. The switching states and associated current paths are shown in Figure 4.10.

Both transistors turn on at zero voltage yet experience hard switched turn off transitions. Neither

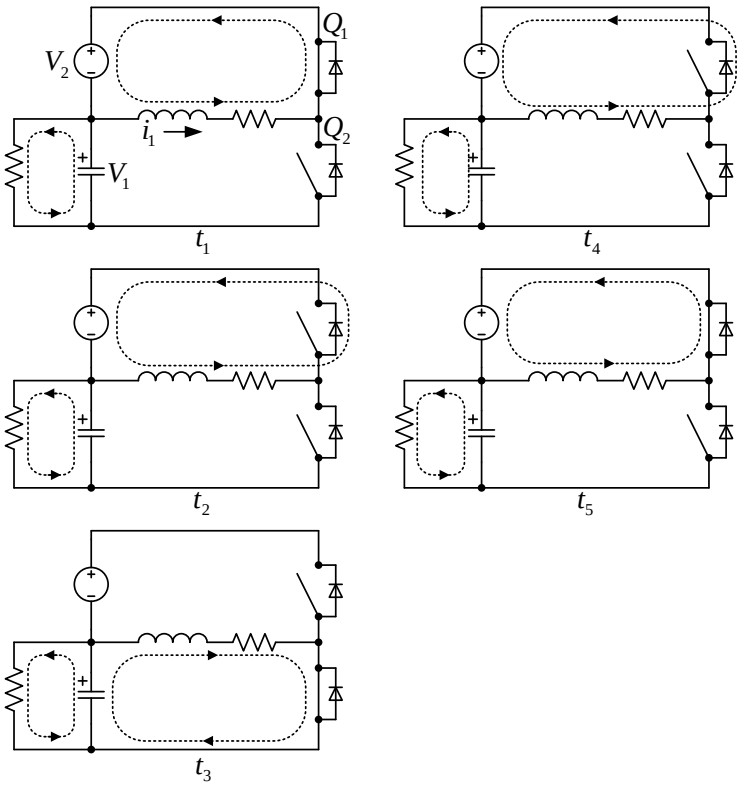


Figure 4.8: Buck Boost Inductor Current Positive at Both Transitions

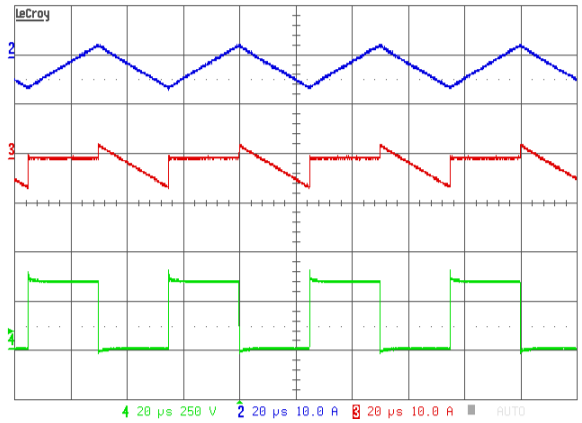


Figure 4.9: Experiment Results of Inductor Current (trace 2), $Q_2$ Current (trace 3), and $Q_2$ Voltage (trace 4) with Positive and Negative Current Transitions

of the diodes experience reverse recovery losses in this mode.

$$I_{Q_1\_on} = I_{Q_2\_off} = I_1 - \frac{\Delta I_1}{2} \tag{4.19}$$

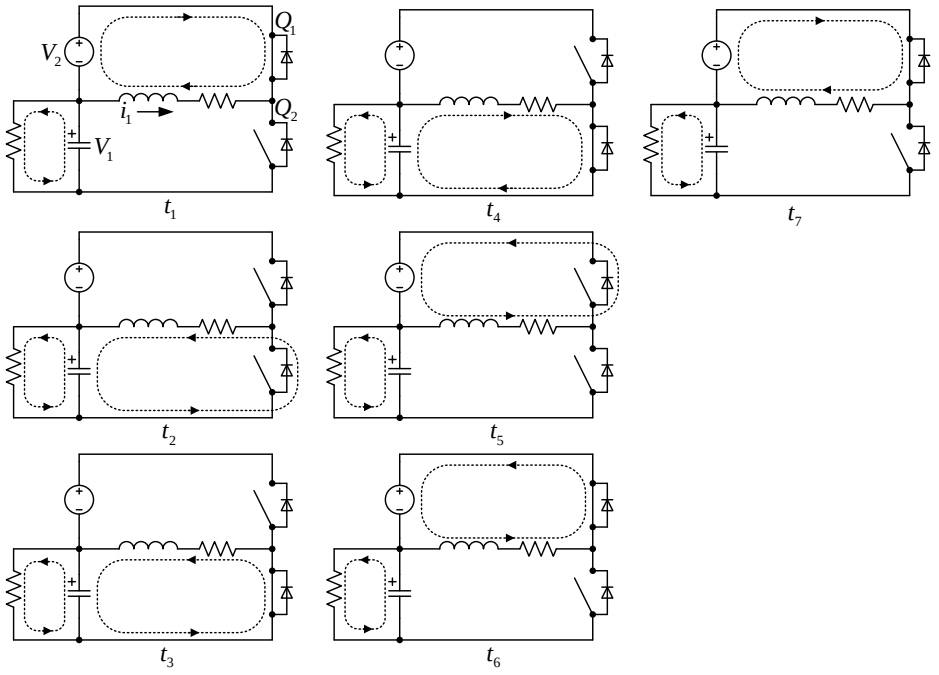


Figure 4.10: Buck Boost Switch States with Both Positive and Negative Transitions

$$I_{Q_{1\_off}} = I_{Q_{2\_on}} = I_1 + \frac{\Delta I_1}{2} \tag{4.20}$$

$$V_{Q_{1\_on}} = V_{Q_{2\_on}} \approx 0 \tag{4.21}$$

$$V_{Q_{1\_off}} = V_{Q_{2\_off}} = V_1 + V_2 \tag{4.22}$$

The last case is similar to the first with opposite current direction. Figure 4.11 shows the current waveform from experiment.

Figure 4.12 illustrates the switching sequence. The bottom side transistor ($Q_2$) experiences ZVS at both transitions.

$$I_{Q_{1\_on}} = I_{Q_{2\_off}} = I_1 - \frac{\Delta I_1}{2} \tag{4.23}$$

$$I_{Q_{1\_off}} = I_{Q_{2\_on}} = I_1 + \frac{\Delta I_1}{2} \tag{4.24}$$

$$V_{Q_{1\_on}} = V_{Q_{1\_off}} = V_1 + V_2 \tag{4.25}$$

$$V_{Q_{2\_on}} = V_{Q_{2\_off}} \approx 0 \tag{4.26}$$

In practical closed loop operation when the PV array is feeding current, the average buck boost inductor current is negative and equal to the input current. Furthermore the current includes a double

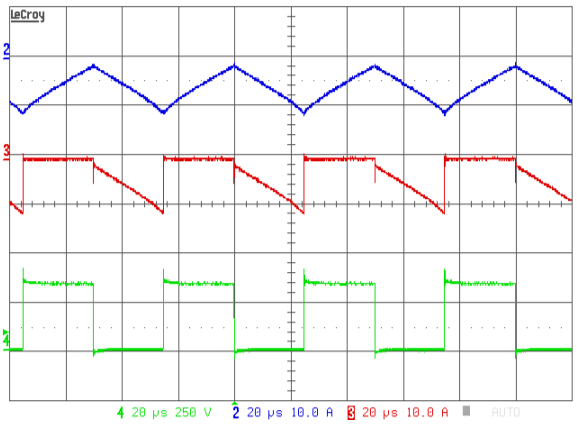


Figure 4.11: Experiment Results of Inductor Current, $Q_2$ Current, and $Q_2$ Voltage with Negative Current Transitions

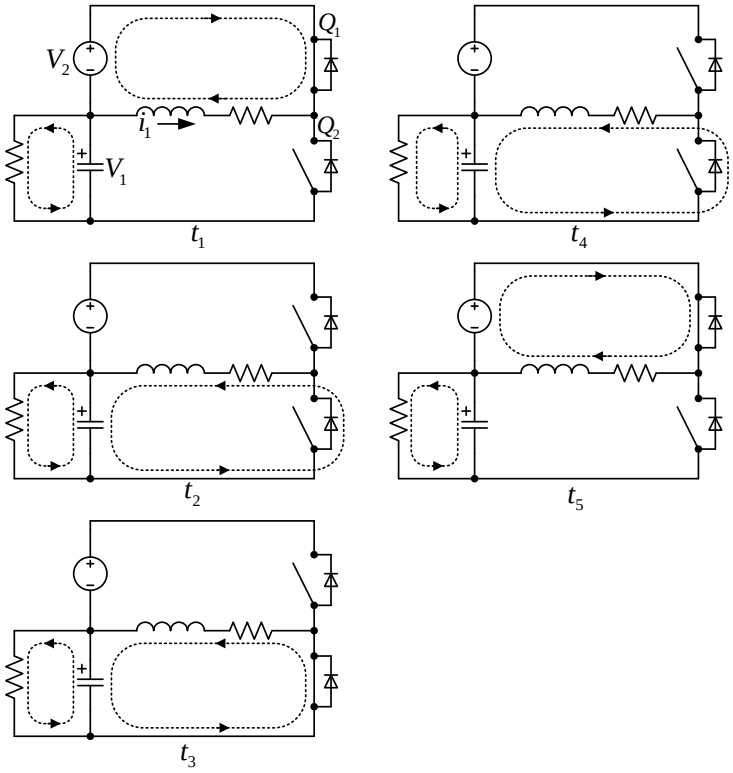


Figure 4.12: Buck Boost Inductor Current Negative at Both Transitions

line frequency component as illustrated in Figure 4.13. Thus the circuit is usually operating in case three (predominantly negative current).

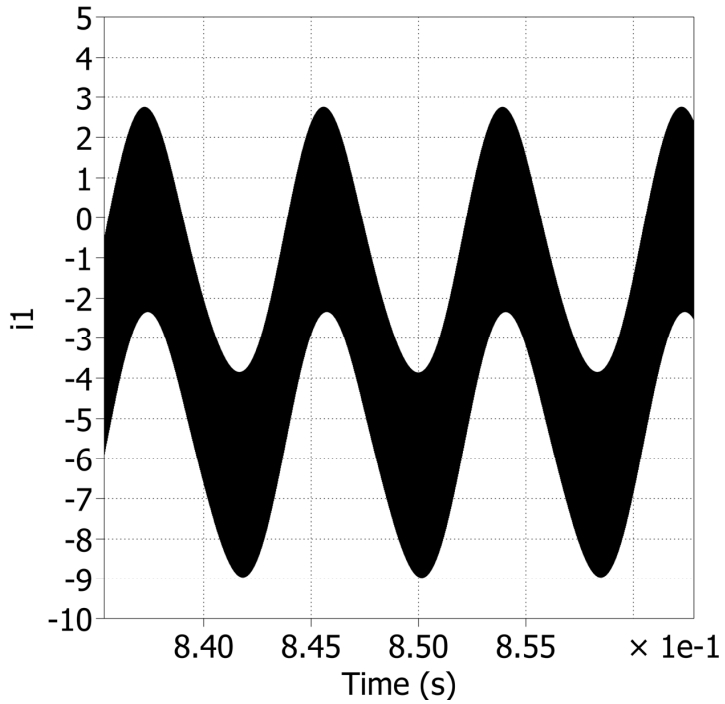


Figure 4.13: Buck Boost Inductor Current Under Normal Operating Condition

### 4.3.3 Buck Boost Switching Losses

Once the operating mode has been identified, the corresponding instantaneous currents and voltages at transition instant can be determined. With the transition voltages/currents, the transition energies can be found.

Reverse recovery energy is also dissipated when diodes transition from conducting to blocking current [54]. The reverse recovery charge $(Q_c)$ is usually provided in the data sheet and from this, the recovery energy can be found.

$$E_{diode} = Q_c V_{ds} \tag{4.27}$$

Furthermore, energy is dissipated in the gate drive circuit. Once again this energy can be found as a change of stored charge [53]. The drive voltage is represented in (4.28) as $V_g^+$ and $V_g^-$ for positive and negative states respectively.

$$E_{drive} = Q_g * (V_{g^+} - V_{g^-}) \tag{4.28}$$

Finally the net average switching power loss per device is the product of total transition energy

dissipated and switching frequency.

$$P_{sw} = (E_{on} + E_{off} + E_{diode} + E_{drive}) f_{sw} \tag{4.29}$$

## 4.4 Inverter Semiconductor Losses

This section presents investigations of switching and conduction losses for the split phase inverter of Figure 1.18. This method is borrowed from [55].

The average duty signals of the inverter power pole transistors have both DC and AC components. $M \in [0, .5]$ is the modulation index, $\Theta = \omega t$ is the instantaneous phase angle, and $\Phi$ is the phase angle displaced term relative to the inductor current.

$$d_2 = \frac{1}{2}\left(1 + M\sin(\Theta + \Phi)\right) \tag{4.30}$$

$$d_3 = \frac{1}{2}\left(1 - M\sin(\Theta + \Phi)\right) \tag{4.31}$$

It is also assumed the average inverter inductor current is sinusoidal.

$$i_2 = I_g \sin(\Theta) \tag{4.32}$$

### 4.4.1 Inverter Conduction Losses

The first step in determining conduction losses is to find the RMS current. Over one fundamental cycle, the RMS current is as follows.

$$I_{Q3\_rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_2^2 d_3 d\Theta} \tag{4.33}$$

After inserting 4.31 and 4.32 into 4.33 and simplifying, the RMS current is found to be independent of displacement angle and modulation index.

$$I_{Q3\_rms} = \sqrt{\frac{I_g^2}{4}} \tag{4.34}$$

The conduction power dissipated in one of the transistors is then just a function of RMS current and on state resistance.

$$P_{Q3} = R_{ds} I_{Q3\_rms}^2 = \frac{R_{ds} I_g^2}{4} \tag{4.35}$$

Each transistor experiences the same power dissipation, thus the net conduction loss for both split phase inverters is:

$$P_{cond} = R_{ds} I_g^2 \tag{4.36}$$

### 4.4.2 Inverter Switching States

The switching sequence for both half bridge inverters is show in Figure 4.14 for a balanced operating mode and positive current in $L_2$. Diagonal transistor pairs are essentially conducting at the same time.

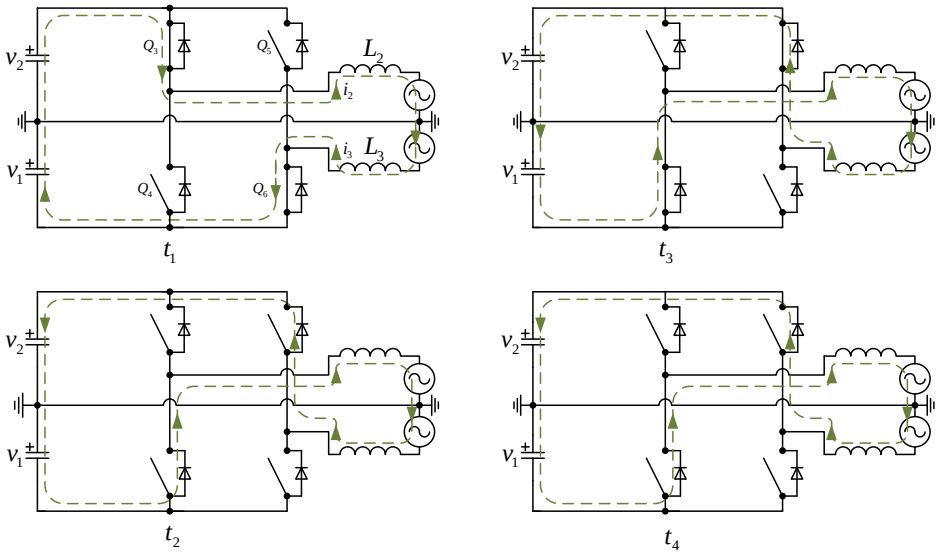


Figure 4.14: Split Phase Inverter Switching States and Currents in Balanced Operation

### 4.4.3 Inverter Switching Losses

The switching losses are approximated here in a similar manner as in [51], [55], and [56]. The switching losses are found by averaging the high frequency average power loss over half the fundamental wave.

$$P_{sw} = \frac{1}{\pi}\int_0^{\pi} f_s E_{tot}(i)\, d\Theta \tag{4.37}$$

Where $E_{tot}$ is the polynomial expression for the sum of turn on and turn off switching energies as a function of instantaneous current: (4.1) or (4.2). The high frequency average switching power dissipated over a switching cycle is the product of the total transition energy $E_{tot}$ and the switching frequency. Combining (4.37), (4.32), and (4.1) gives the long term average power dissipated as a function of switching frequency and peak current.

$$P_{sw} = \frac{1}{\pi}\int_0^{\pi} f_s \left(aI_g^2 \sin^2(\Theta) + bI_g \sin(\Theta) + c\right) d\Theta = \frac{f_s(\frac{aI_g^2\pi}{2} + 2bI_g + c\pi)}{\pi} \tag{4.38}$$

The total inverter switching power dissipated is only two times this because at any instant two of the transistors are soft switched. It can be noted from Figure 4.14 that $Q_4$ and $Q_5$ experience ZVS. This is because the transistor's body diodes are forward biased before and after the device is switched. Similarly when the current is negative in $L_2$, $Q_3$ and $Q_6$ will experience ZVS.

## 4.5 Power Semiconductor Thermal Analysis

The thermal analysis here is common approximation technique where the thermal system is modeled as an electric circuit [57]. Temperature is analogous to voltage, power is analogous to current, and thermal mass behaves like a capacitor with units of energy/temperature. Thermal resistance has units of temperature/power.

The Cauer representation of the thermal circuit [58], illustrated in Figure 4.16, approximates thermal dynamic behaviour. The power dissipated in each semiconductor is represented by the current sources $i_1 - i_6$. The network includes junction to case resistances $R_{JC}$, case thermal capacitances $C_C$, case to heat sink resistances $R_{CS}$, heat sink thermal capacitance $C_S$, and heat sink to ambient temperature resistance $R_{SA}$. It is important to note that the ground in this circuit is actually ambient temperature so the voltages just represent temperature rise. The parameters utilized in the implementation are listed in Table 4.3. The values were obtained from the data sheets provided by the manufacturers of the semiconductors, insulators, and heat sinks. The units were adjusted as necessary to represent the actual thermal system of Figure 4.16.

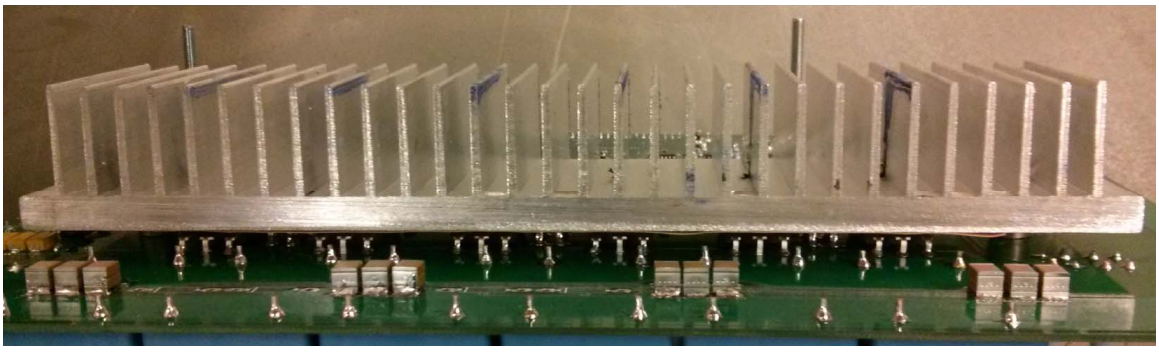

Figure 4.15: Thermal System to be Investigated

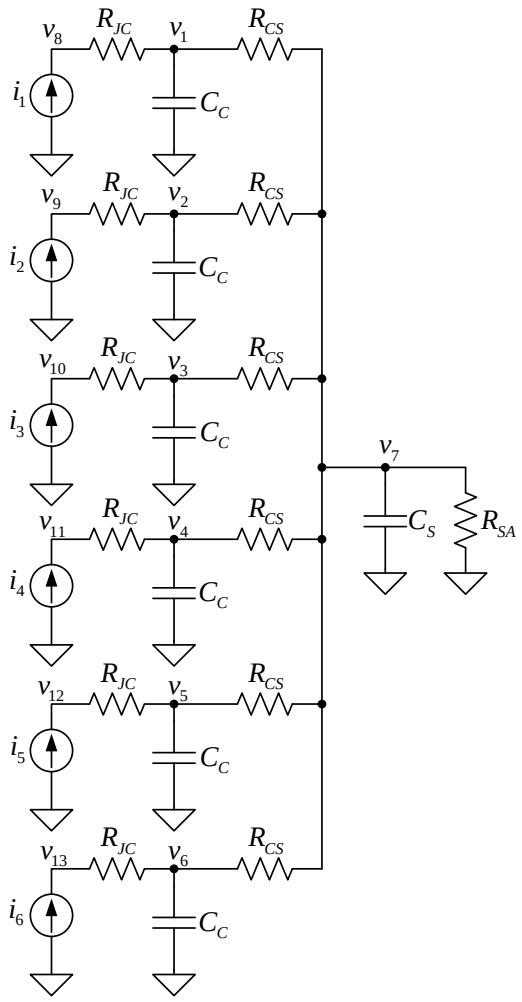


Figure 4.16: Thermal Model Network Approximation

Table 4.3: Parameters for Thermal Analysis

| **DESCRIPTION** | **SYMBOL** | **VALUE** |
|---|---|---|
| Cree CMF10120D | $R_{JC}$ | $.66\ C°/W$ |
| Cree CMF10120D | $C_C$ | $1.57\ J/C°$ [59] |
| Wakefield 1703 (2" segment) | $R_{SA}$ | $1.4\ C°/W$ |
| Wakefield 1703 (2" segment) | $C_S$ | $416.2\ J/C°$ |
| Bergquist SIL-PADK10 (50 PSI and TO-247 package) | $R_{CS}$ | $.807\ C°/W$ |

The circuit is a linear system; the outputs are the voltages (junction temperatures) at each power semiconductor.

$$\begin{bmatrix} \dot{v_1} \\ \dot{v_2} \\ \dot{v_3} \\ \dot{v_4} \\ \dot{v_5} \\ \dot{v_6} \\ \dot{v_7} \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_{CS}C_C} & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{CS}C_C} \\ 0 & \frac{-1}{R_{CS}C_C} & 0 & 0 & 0 & 0 & \frac{1}{R_{CS}C_C} \\ 0 & 0 & \frac{-1}{R_{CS}C_C} & 0 & 0 & 0 & \frac{1}{R_{CS}C_C} \\ 0 & 0 & 0 & \frac{-1}{R_{CS}C_C} & 0 & 0 & \frac{1}{R_{CS}C_C} \\ 0 & 0 & 0 & 0 & \frac{-1}{R_{CS}C_C} & 0 & \frac{1}{R_{CS}C_C} \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_{CS}C_C} & \frac{1}{R_{CS}C_C} \\ \frac{1}{R_{CS}} & \frac{1}{R_{CS}} & \frac{1}{R_{CS}} & \frac{1}{R_{CS}} & \frac{1}{R_{CS}} & \frac{1}{R_{CS}} & -\left(\frac{6}{R_{CS}} + \frac{1}{R_{SA}}\right) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \end{bmatrix} + \begin{bmatrix} \frac{1}{C_C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_C} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_C} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_C} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_C} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} \tag{4.39}$$

$$\begin{bmatrix} v_8 \\ v_9 \\ v_{10} \\ v_{11} \\ v_{12} \\ v_{13} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \end{bmatrix} + \begin{bmatrix} R_{JC} & 0 & 0 & 0 & 0 & 0 \\ 0 & R_{JC} & 0 & 0 & 0 & 0 \\ 0 & 0 & R_{JC} & 0 & 0 & 0 \\ 0 & 0 & 0 & R_{JC} & 0 & 0 \\ 0 & 0 & 0 & 0 & R_{JC} & 0 \\ 0 & 0 & 0 & 0 & 0 & R_{JC} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} \tag{4.40}$$

The system was solved with the circuit at full power and at a worst case PV voltage. The plot of Figure 4.17 shows how the junction temperature of each semiconductor increases as the heat sink warms up. It can be seen the junction temperature is well below the maximum permitted $125°C$.

## 4.6 Core Losses with Steinmetz Method

Predicting performance of power converter magnetic components is difficult, especially if performance plots are not available. In particular the core losses are rather complicated. According to [60], common techniques to model the core losses include the Steinmetz equation, a loss map from measurements, hysteresis models, and analytic separation of eddy current and hysteresis components.

The empirical method used here is the Steinmetz equation (4.41) [60]. This equation groups the hysteresis and eddy current losses together. The equation gives power loss per unit volume $(P_v)$ in units of $mW/cm^2$ as a function of peak flux density in $kG$ and frequency in $kHz$. The constants $\gamma$, $\alpha$, and $\beta$

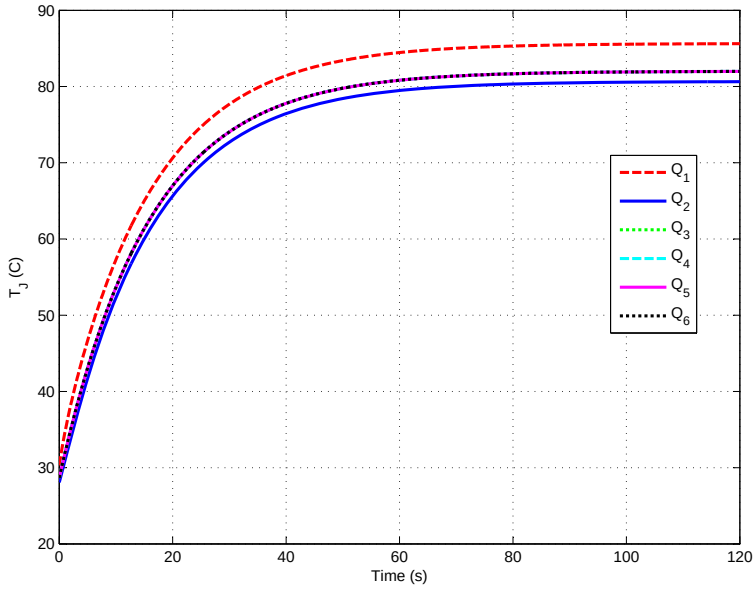


Figure 4.17: Junction Temperature of Each Power Semiconductor

may be determined from measurements as described later or from the manufacturer's data sheet.

$$P_v = \gamma f^{\alpha} \hat{B}^{\beta} \tag{4.41}$$

This equation is however only valid for sinusoidal waveforms. The Modified Steinmetz Equation (MSE) [61] is a variation to accommodate non-sinusoidal waveforms. This reference identifies an "average rate of remagnitization" rather than frequency as the key parameter of core losses. The equivalent frequency is then a function of the average change in flux density squared over one switching cycle. Where $\Delta B = B_{max} - B_{min}$.

$$f_{eq} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left( \frac{dB}{dt} \right)^2 dt \tag{4.42}$$

For a basic triangular waveform centered about zero as in Figure 4.9, the equivalent frequency is as follows.

$$f_{eq} = \frac{8}{\pi^2 T} \tag{4.43}$$

The power per volume $(P_v)$ is a function of this equivalent frequency and the waveform frequency. The constants are the same Steinmetz parameters from the sinusoidal version (4.41).

$$P_v = f\left(\gamma f_{eq}^{\alpha-1} \hat{B}^{\beta}\right) = \frac{\gamma}{T} \left( \frac{8}{\pi^2 T} \right)^{\alpha-1} \hat{B}^{\beta} \tag{4.44}$$

The peak flux density for square wave excitation can be found from Faraday's law.

$$\hat{B} = \frac{10^8 V_{on} T}{2AN} = \frac{10^8 V_{on} d}{2AN f_{sw}} \tag{4.45}$$

Where $\hat{B}$ is the peak flux density in Gauss, $V_{on}$ is the voltage applied across the coil, $N$ is the number of turns, $A$ is cross sectional area in $cm^2$. $T$ is the length of time in seconds for which the voltage is applied.

Unfortunately the Steinmetz parameters are not constant as the DC bias of flux density changes. As previously illustrated in Figure 4.13, the DC bias is not constant in this application. Reference [61] investigates the effect of DC bias and indicates this is an open problem to be solved. One possible way to accommodate DC bias is to modify the non exponent Steinmetz parameter for various premagnetization points [61].

## 4.7 Identifying Steinmetz Parameters

The modified Steinmetz equation (4.44) requires parameters from the sinusoidal version. These can be found from measurements. The details are explained here.

First an accurate measurement setup as described in [62] is required. This includes a power amplifier to energize the core, an accurate current and voltage sensor to measure power fed to the circuit, and a voltage sense winding to measure flux density.

At several frequencies the flux density should be swept and average input power measured at each point. The $\beta$ exponent of (4.41) can be found from two different flux density data points at a constant frequency.

$$\beta = \frac{log(P_2) - log(P_1)}{log(B_2) - log(B_1)} \tag{4.46}$$

Next the excitation voltage should be held constant while the frequency is varied. The $\alpha$ exponent can be found from two different frequency measurements at a constant flux density.

$$\alpha = \frac{log(P_2) - log(P_1)}{log(f_2) - log(f_1)} \tag{4.47}$$

Finally the constant $\gamma$ can be found from from a third data point after the other constants have been determined.

$$\gamma = \frac{P}{f^{\alpha} \hat{B}^{\beta}} \tag{4.48}$$

## 4.8 Characteristics of Selected Inductor

A powdered iron inductor core from Micrometals (E450-2) was selected for both the buck boost converter and inverter sections of the power circuit. This core is a bit oversized and was chosen to provide reduced peak flux density and in turn reduced core losses. Important characteristics of the inductor are listed in Table 4.4.

Table 4.4: Parameters for Micrometals E450-2 Inductor Core

| **DESCRIPTION** | **SYMBOL** | **VALUE** |
|---|---|---|
| Inductance factor | $A_L$ | $132\ nH/N^2$ |
| Length of flux path | $l$ | $22.9\ cm$ |
| Cross sectional area | $A$ | $12.2\ cm^2$ |
| Core volume | $V$ | $280\ cm^3$ |
| Number of turns | $N$ | $70$ |
| Core loss parameter | $a$ | $4 * 10^9$ |
| Core loss parameter | $b$ | $3 * 10^8$ |
| Core loss parameter | $c$ | $2.7 * 10^6$ |
| Core loss parameter | $d$ | $8 * 10^{-15}$ |

Micrometals provides a curve fit equation for this material to approximate core loss as a function of peak flux density $(\hat{B})$. This is called the Oliver model [63], and is somewhat like the Steinmetz equation but with separate terms for hysteresis and eddy current losses. The equation is plotted in Figure 4.18 for the selected inductor at 50% duty and various input voltages.

$$P_v = \frac{f}{\frac{a}{\hat{B}^3} + \frac{b}{\hat{B}^{2.3}} + \frac{c}{\hat{B}^{1.65}}} + df^2\hat{B}^2 \tag{4.49}$$

The inductor was wound with $70$ turns to give a net inductance of about $647\ \mu H$. The same inductor configuration was also used for the inverters.

## 4.9 Buck Boost Inductor Losses

The buck boost inductor losses are a result of both power dissipated in the copper wire and power dissipated in the magnetic core.

### 4.9.1 Buck Boost Conduction Losses

The copper wire losses can be found by approximating the wire with an equivalent series resistance. If the inductor is wound with sufficiently small strands, only DC resistance is needed. If not, the AC resistance should be identified. In this particular application, litz wire with $235$ strands of $36$ gauge wire was utilized.

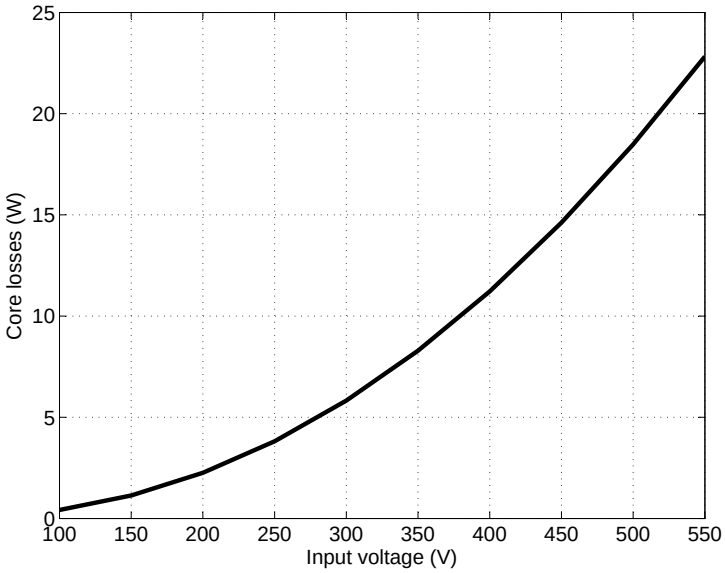


Figure 4.18: Oliver Core Loss Model of Selected Inductor

Equations for the average DC offset ($I_1$) and peak to peak ripple ($\Delta I_1$) are listed here. The current direction reference is from Figure 3.5. DC link currents drawn by the inverter are given the symbol $I_{inv}$.

$$I_{inv} = \frac{P_{in}}{V_1 + V_2} \tag{4.50}$$

$$I_1 = -\frac{I_4 - I_{inv}}{D_1} = -\frac{(I_4 - I_{inv})}{\left(\frac{V_1}{V_1+V_2}\right)} \tag{4.51}$$

$$\Delta I_1 = \frac{V_1 V_2}{(V_1 + V_2) f_{sw} L_1} \tag{4.52}$$

Current in the buck boost converter is triangular with a DC offset. The RMS current of such a wave-shape is a function of the average and peak-peak current ripple [64].

$$I_{1\_rms} = \sqrt{I_1^2 + \left(\frac{\Delta I_1}{2\sqrt{3}}\right)^2} \tag{4.53}$$

The conduction power dissipated can then be found from Watts law.

$$P_{L1\_cop} = I_{1\_rms}^2 R_1 \tag{4.54}$$

### 4.9.2 Buck Boost Core Losses

The buck boost core losses are fairly straight forward. The peak flux density over a switching cycle is a function of link voltages, switching frequency, and inductor parameters.

$$\hat{B} = \frac{10^8 \left(\frac{V_2 V_1}{V_2 + V_1}\right)}{2ANf_{sw}} \tag{4.55}$$

This can then be inserted into (4.49) to attain a closed form core loss equation for the buck boost converter.

## 4.10 Inverter Inductor Losses

The inverter inductor losses are a result of both power dissipated in the copper wire and power dissipated in the magnetic core.

### 4.10.1 Inverter Conduction Losses

Conduction losses of the buck boost converter can be found from Watts law using the RMS current and DC wire resistance.

### 4.10.2 Inverter Core Losses

The inverter core losses are evaluated in a slightly different approach than for the buck boost converter. Specifically it will be shown how variable grid voltage causes the switching frequency core losses to be significantly reduced. This analysis is essentially following the approach in [65]. The discussion will be in context of $L_2$ from the following image. The duty signal ($d_2$) can vary from zero to one.

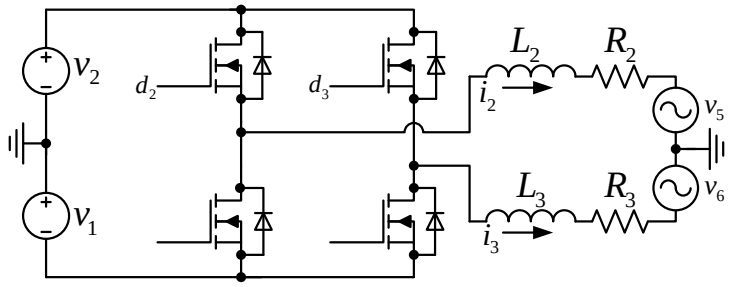


Figure 4.19: Inverter Power Circuit

The instantaneous voltage across the inductor is the difference between the DC link voltage and grid voltage: $v_{L2} = V_2 - v_5$. Also the instantaneous grid voltage is about equal to the control voltage and so the duty is approximately as follows.

$$d_2 \approx \frac{v_5 + V_1}{V_2 + V_1} \tag{4.56}$$

Inserting these relationships into Faraday's equation (4.45) gives the peak flux density as a function of instantaneous grid voltage ($v_5$).

$$\hat{B} = \frac{10^8 (V_2 - v_5) \left( \frac{v_5 + V_1}{V_2 + V_1} \right)}{2ANf_{sw}} \tag{4.57}$$

The peak flux density can then be inserted into the power loss equation (4.49) to show how instantaneous power is dissipated over a fundamental period. The ripple current and flux density changes throughout a fundamental cycle. The maximum peak flux density occurs when the duty is one half; this corresponds to zero average output voltage. Figure 4.20 illustrates these waveforms and the average power dissipated in the inverter cores.

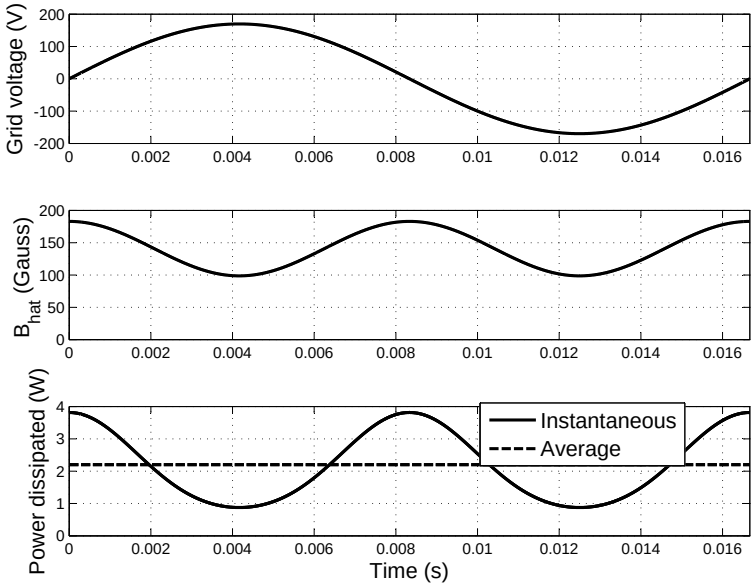


Figure 4.20: Instantaneous and Average Core Losses of Inverter Inductor

## 4.11 Frequency Dependence of Efficiency

The net converter efficiency is dependent on the switching frequency because transistor switching and inductor core losses are frequency dependent. From equation (4.29) illustrated in Figure 4.21

it is obvious switching losses increase with increased frequency. However the core losses reduce as frequency increases. This is because the peak flux density reduces with increased frequency. A plot of equation (4.49) that includes frequency dependent flux density (4.55) is illustrated in Figure 4.22.

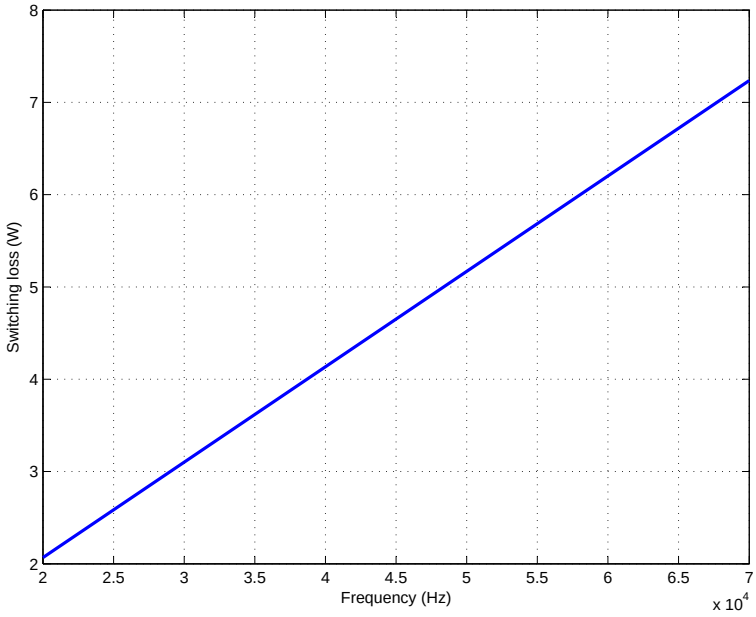


Figure 4.21: Switching Losses of Buck Boost Converter as Function of Frequency

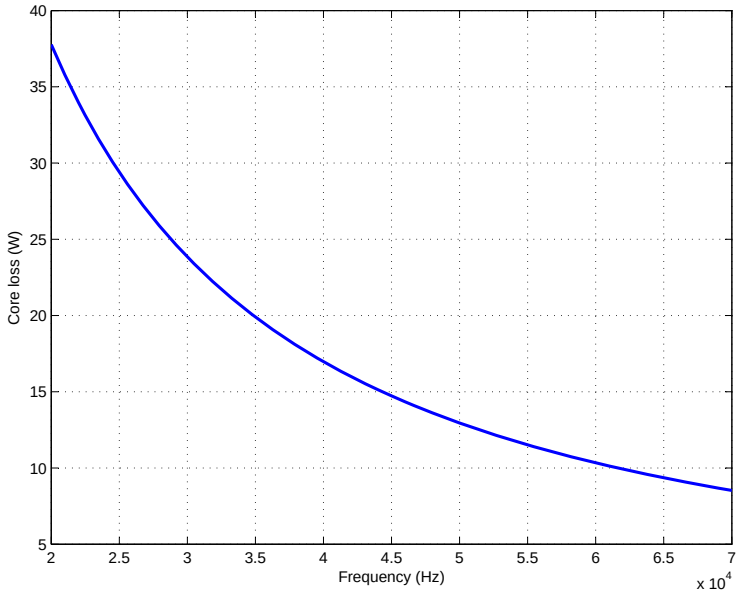


Figure 4.22: Core Losses as a Function of Frequency

An experiment was conducted to find an optimal switching frequency. The converter of Figure 2.1 was run open loop with the buck boost duty ratio at 50%. The modulation index of both inverters was set constant at $.34$. LC filters and resistive loads of about $24\ \Omega$ were placed at the output of each inverter. The input voltage was ramped from $200V$ to $475V$. At the maximum input voltage the circuit was supplying approximately rated power of $1kW$. The experiment was repeated at five different frequencies and efficiency was measured at each operating point. The results shown in Figure 4.23 indicate the optimal frequency is $40\ kHz$ with an average efficiency of $95.3\ \%$. It should be noted that the accuracy of this particular experiment is rather poor.

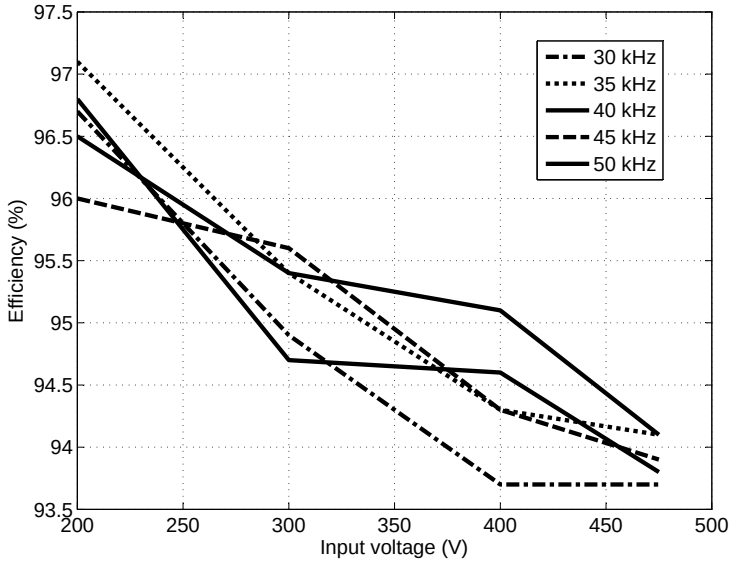


Figure 4.23: Measured Efficiency as Function of Input Voltage for Several Switching Frequencies

## 4.12 Complete Efficiency

The net efficiency ($\eta$) was evaluated analytically at a switching frequency of $40\ kHz$.

$$\eta = \frac{P_{in} - P_{diss}}{P_{in}} \tag{4.58}$$

Where $P_{diss}$ is the sum of power dissipated in inductors and semiconductors.

$$P_{diss} = P_{L1} + P_{L2} + P_{L3} + P_{Q1} + P_{Q2} + P_{Q3} + P_{Q4} + P_{Q5} + P_{Q6} \tag{4.59}$$

Figure 4.24 shows the analytic prediction of efficiency. Figure 4.25 illustrates power dissipated in each component at a particular operating condition. The buck boost inductor has the greatest dissipation

because of the large RMS current through the component. The buck boost transistor $Q_2$ is dissipating the least power because it is mostly soft switched.

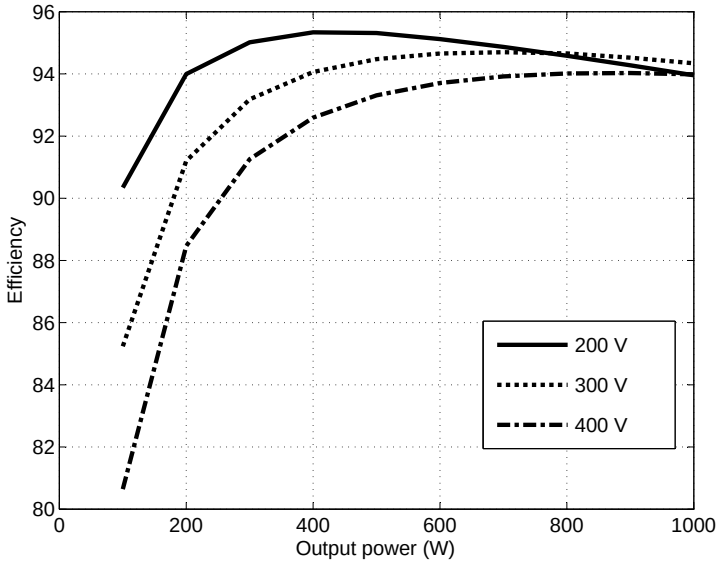


Figure 4.24: Predicted Efficiency at Various Input Voltages

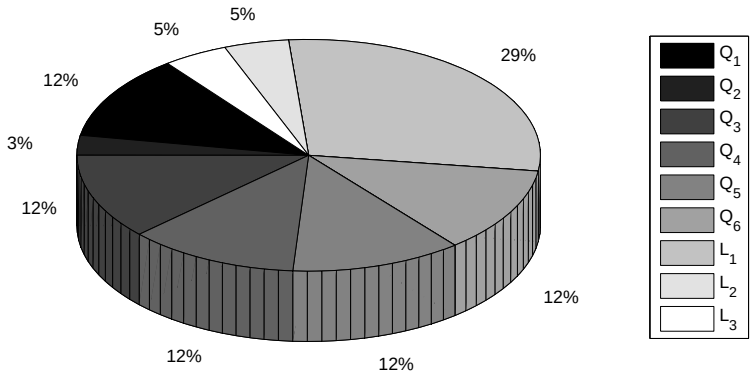


Figure 4.25: Power Dissipated in Various Components with $V_1 = 250\,V$ and $V_2 = 200\,V$

# Chapter 5

# SIMULATIONS

Many simulations were conducted using Plexim PLECS toolbox within the Matlab/Simulink environment. The simulated circuit was configured to match the actual hardware experiment as close as possible. A script as in [66] was configured to assist in the development process and load appropriate systems and constants into the Matlab workspace.

The purpose of these simulations was first and foremost to ensure basic functionality under a variety of conditions. This included validation of the control systems, and component stress. The inverter and buck boost converter were each evaluated separately, then combined as a single system. The converter was evaluated at minimum and maximum input voltages and at zero and full power. Most of the simulations entailed relatively slow voltage or power ramps. A few results are presented and discussed here.

## 5.1 Buck Boost Converter Simulated

The buck boost converter was first simulated in closed loop operation separate from the inverter section. Figure 5.1 shows the power circuit simulation schematic. The current source $i_x$ represents the disturbance current of the inverter section. Figure 5.2 illustrates the control loop. It is comprised of a basic linear control system to regulate the voltage across the top side capacitor $(v_2)$ while subject to input current disturbances. Figure 5.3 shows the state variables at startup. Control of the input voltage appears to be functioning appropriately. The initial large transient of $v_2$ is caused by initialization of the low pass filter $H_1$. The bottom side capacitor voltage $(v_1)$ is unregulated and settles to an equilibrium after a while. Although not shown in this figure, the control system was also verified in presence of disturbances.

## 5.2 Inverter Simulated

Similarly, the inverter was also simulated as a separate circuit decoupled from the DC-DC converter. The DC link was established with a DC voltage source and the inner current loops were activated. The power circuit and control loops are shown in Figures 5.4 and 5.5 respectively.

Figure 5.6 shows results from one of the phases. The top trace is the grid voltage. The bottom trace shows the phase current superimposed upon the reference. The reference is tracked well with zero steady state error. Although not shown, input disturbance rejection was also verified.

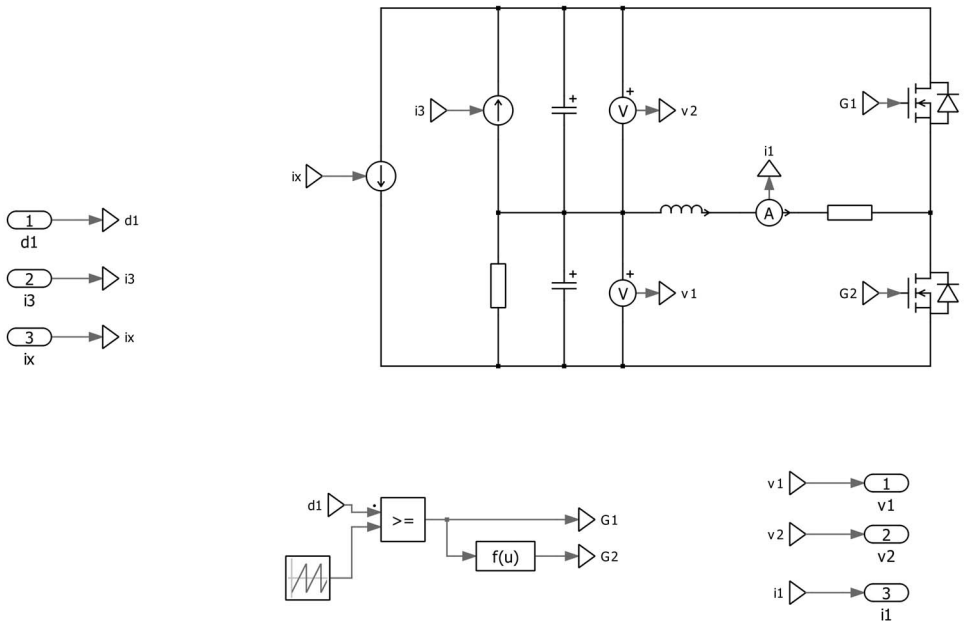


Figure 5.1: Power Circuit of Buck Boost Converter Simulation

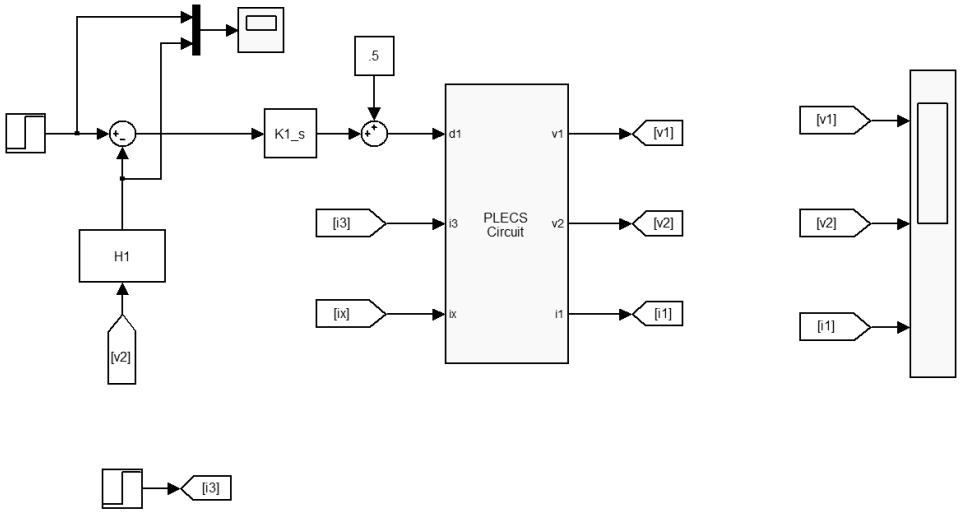


Figure 5.2: Control Loop of Buck Boost Converter Simulation

## 5.3 Complete System Simulated

The complete system was then simulated to evaluate functionality and transient behavior. Figures 5.7 and 5.8 show the power circuit and control loops as configured within the simulation environment.

First startup transient behavior was evaluated. In Figure 5.9 the capacitor voltages are shown

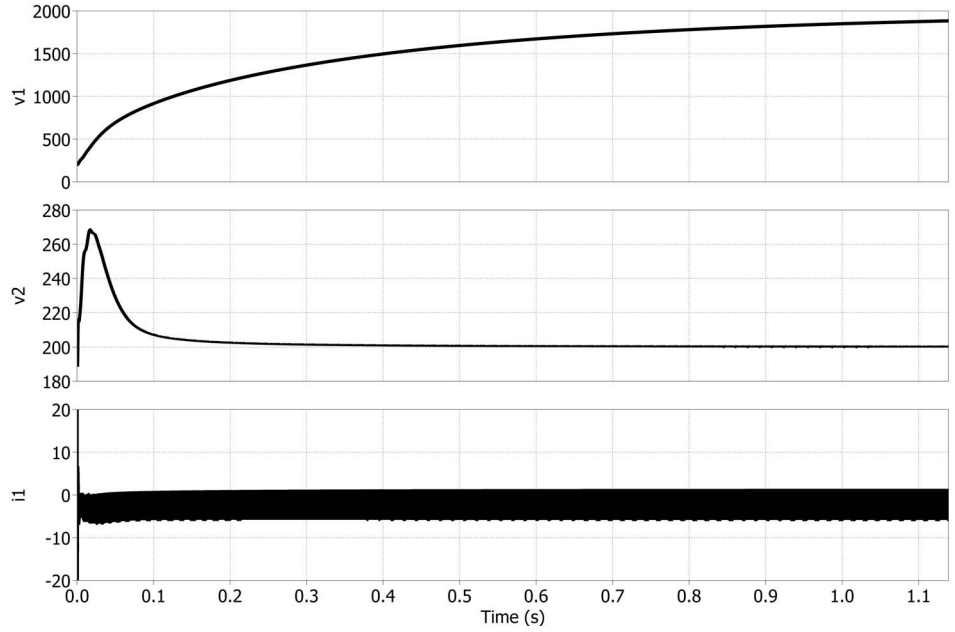


Figure 5.3: Buck Boost Converter Simulation Results

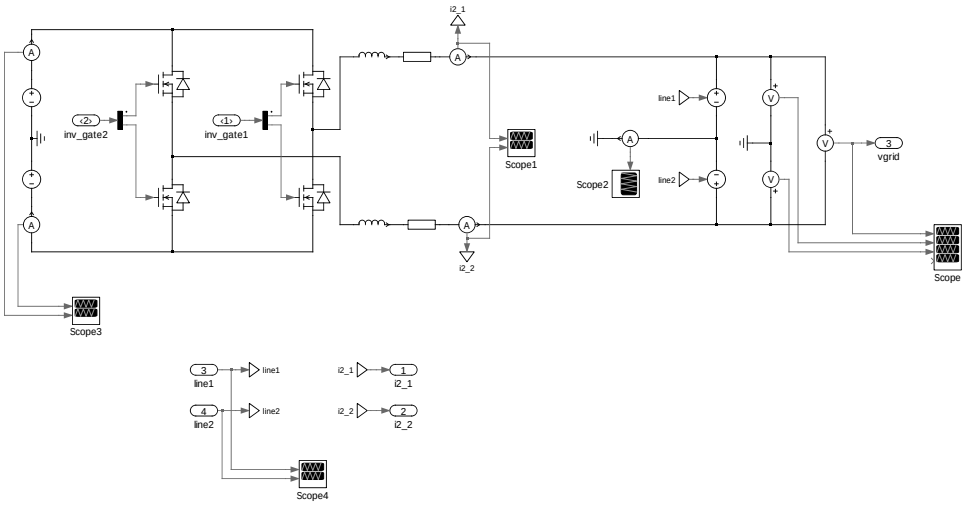


Figure 5.4: Power Circuit of Inverter Simulation

along with average buck boost inductor current, and average grid currents. Initially the circuit is attached to the grid with the buck boost converter running at 50 % duty ratio. At $.1$ seconds, the inverter control system is started to regulate the bottom side capacitor voltage at $200\ V$. At $.3$ seconds, the buck boost controller is activated to regulate the top side capacitor voltage $(v_2)$ equal to the bottom side capacitor voltage. This does not change much because there is no power flowing at that moment. At $.4$ seconds, one amp of input PV current is applied which results in current fed to the grid. The simulation shows

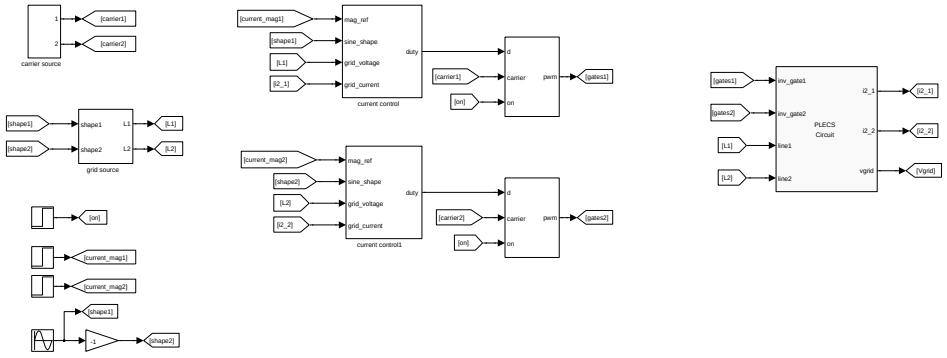


Figure 5.5: Control Loop of Inverter Simulation

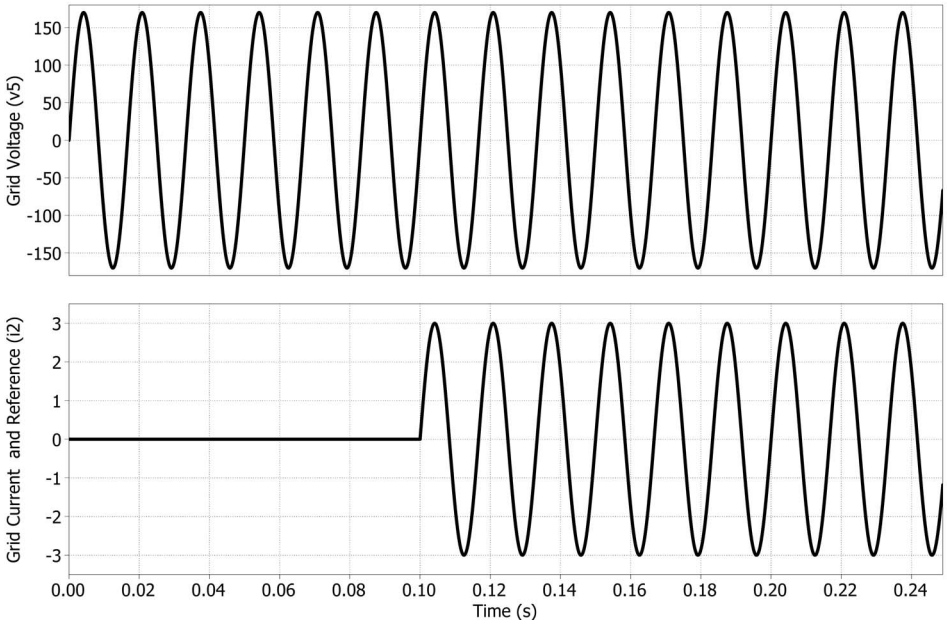


Figure 5.6: Inverter Simulation Results

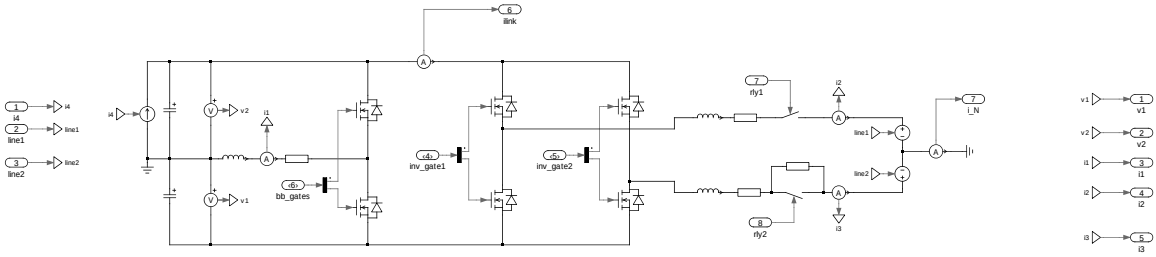


Figure 5.7: Simulation Schematic of Complete Power Circuit

correct functionality. In particular, inrush and controller start up transients are not excessive and also the double line frequency currents are absorbed by $C_1$ only. However, it is also evident the capacitor

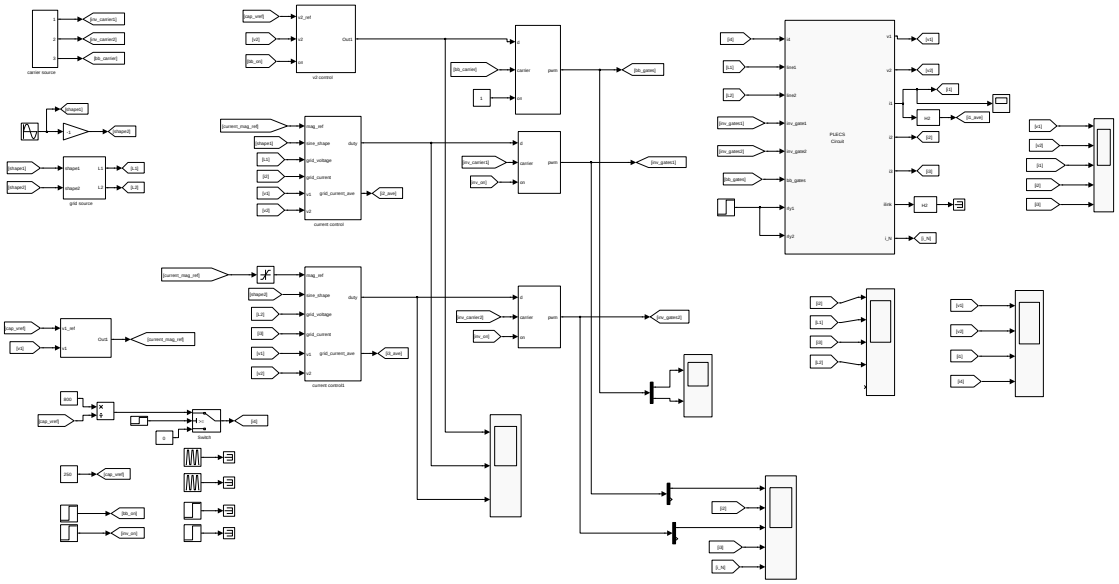

Figure 5.8: Control Loops of Complete System Simulation

voltages are sensitive to stepped current disturbances. This is a result of relatively small capacitance on the DC link and may be an issue with quickly changing solar irradiance.

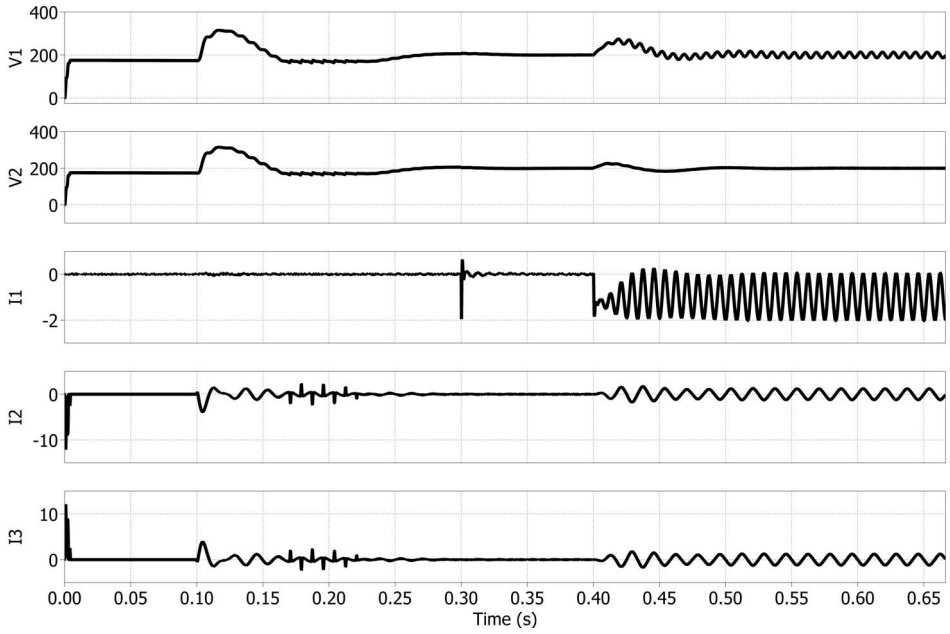


Figure 5.9: Start Up Dynamics of Complete System

In another simulation of the complete circuit, the input voltage is ramped from $200\ V$ to $550\ V$

then back. The bottom side capacitor voltage reference is set equal to the input voltage reference and the input current is held constant at one amp.

Figure 5.10 shows the circuit's average state variables from this simulation. This is a test of the link voltage regulators. Once again the circuit appears to be functioning correctly.

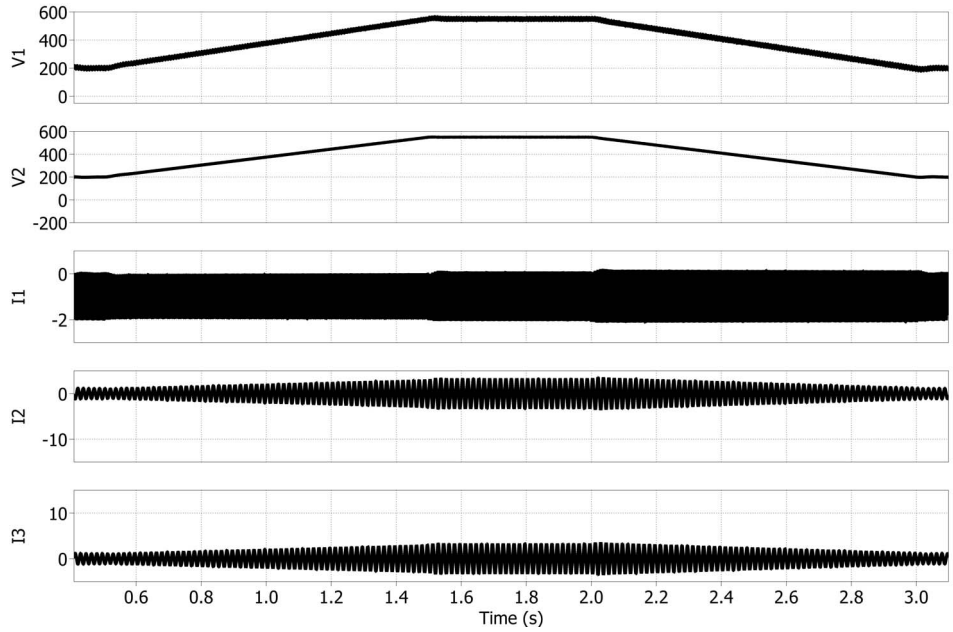


Figure 5.10: Complete System Voltage Ramp Simulation with Constant Input Current

The voltage ramp simulation was repeated although this time with the bottom side capacitor voltage held constant at $200\ V$. This circuit condition is desirable such that the transistors are not exposed to excessive voltages of both DC links at maximum. Time domain plots are shown in Figure 5.11 and the low frequency spectrum is shown in Figure 5.12. The system again appears to functioning appropriately with the grid current spectrum predominately fundamental. This is an important aspect to be evaluated because of possible DC grid currents from an unbalance DC link.

Several other simulations were conducted. Figure 5.13 shows results from the voltage ramp simulation repeated. This time the input power is held constant at $1\ kW$.

Figure 5.14 shows simulation results where the input power is ramped from zero to full power with the DC link voltages held constant. A useful result found from the full power simulations is that the average bottom side capacitor voltage should not be set below $250\ V$.

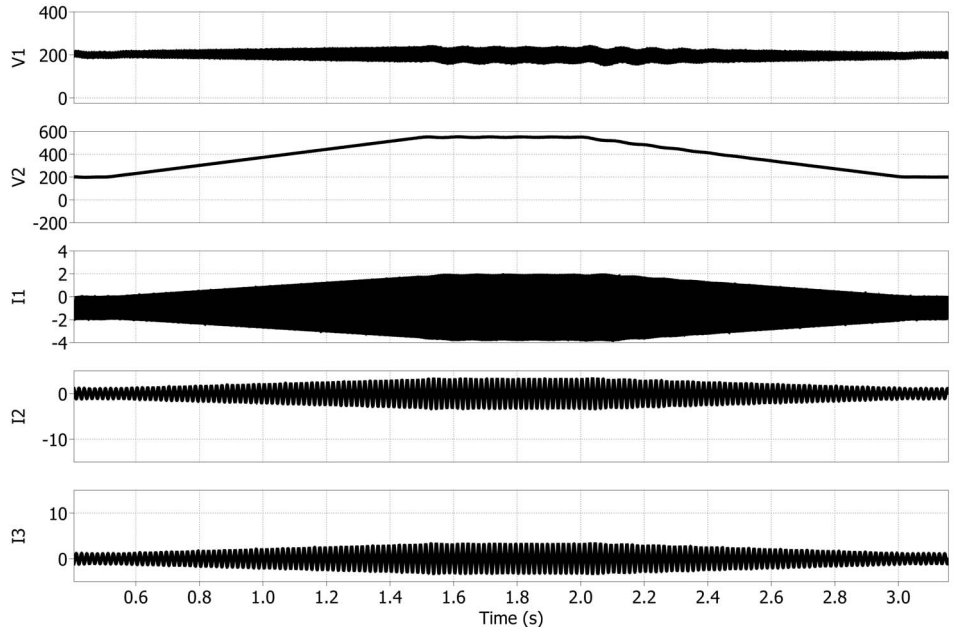


Figure 5.11: Complete System Simulation Results with Bottom Side Capacitor Regulated Constant and Constant Input Current

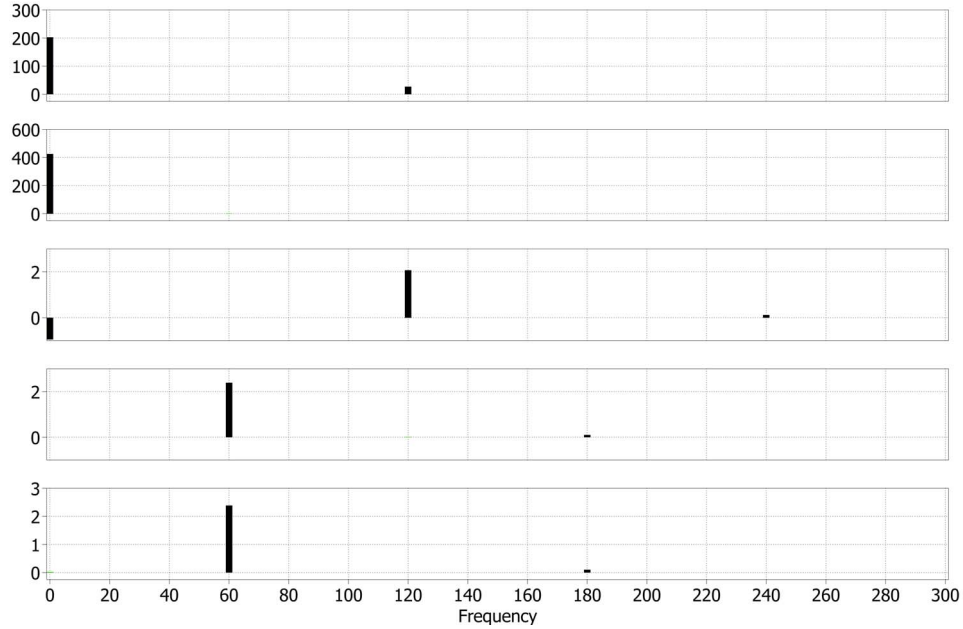


Figure 5.12: Low Frequency Spectrum of State Variables During Ramp Conditions with Unbalanced DC Link

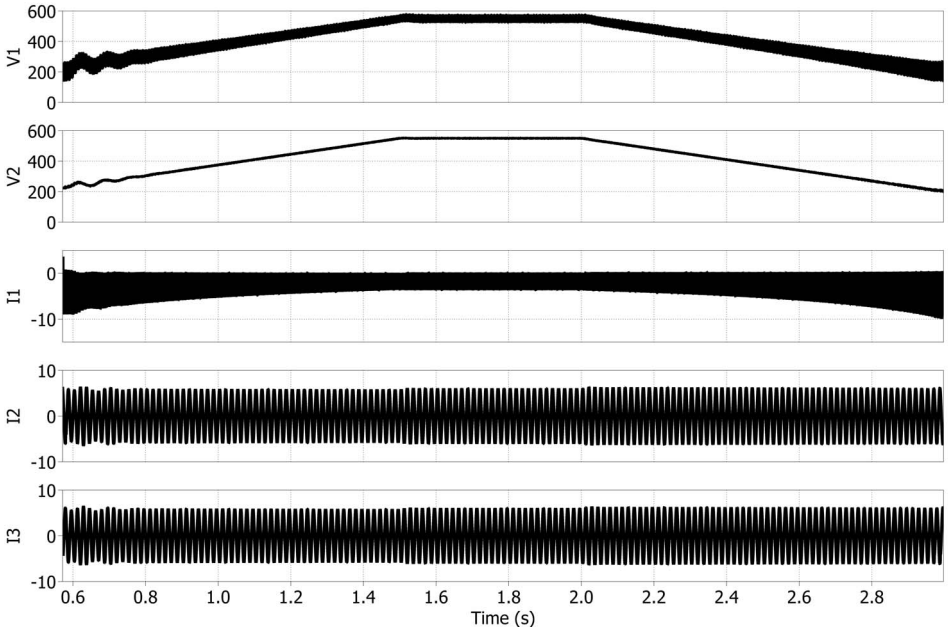


Figure 5.13: Complete System Voltage Ramp Simulation at Constant Full Power

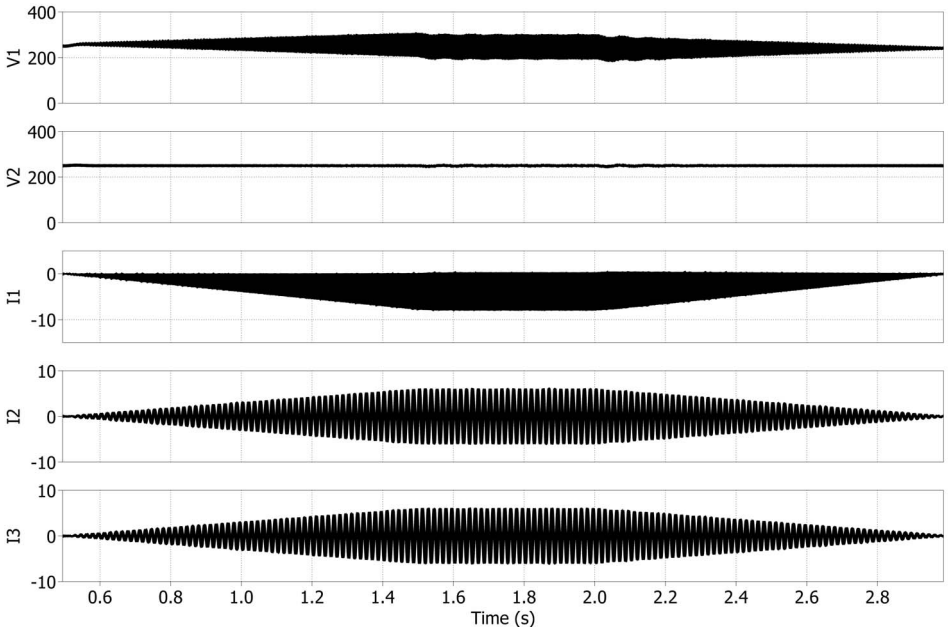


Figure 5.14: Complete System Power Ramp Simulation at Constant Link Voltage

Chapter 6

# IMPLEMENTATION and TEST RESULTS

Finally to prove the concept a hardware prototype was constructed. The target specifications are listed in Table 6.1 below.

Table 6.1: Planned Prototype Specifications

| | |
|---|---|
| Total output power | $1000\,VA$ |
| Output voltage (each phase) | $120\,V_{RMS}$ |
| Output current (each phase) | $4.17\,A_{RMS}$ |
| Efficiency estimate | $96\,\%$ |
| Max input power | $1041.67\,W$ |
| Min input voltage | $200\,V_{DC}$ |
| Max input voltage | $550\,V_{DC}$ |
| Max input current at max input voltage | $1.89\,A_{DC}$ |
| Max input current at min input voltage | $5.21\,A_{DC}$ |

## 6.1 Circuit Boards

A custom power board was drafted for the application. The four layer printed circuit board (PCB) was built with two ounce copper on the outer layers and one ounce copper on the inner layers. A screenshot of the PCB from the drafting software is shown below in Figure 6.1.

The power board includes the power components, gate drive/power supplies, signal conditioning, fault detection, and a wireless communication module. Two ribbon cables link the power board with the control board.

## 6.2 Digital Signal Controller and Firmware

The control system was implemented on a Texas Instruments signal controller (TMS320F28335) with the EZ-DSP development board from Spectrum Digital. This is a floating point processor; however fixed point math libraries were utilized because they were found to be much quicker. The input/output pin map can be found in Appendix B.

The code was developed within TI's Code Composer Studio version 3.3 in the C language. Several different programs were defined using preprocessor directives. The definitions are explained in Table 6.2.

Each block of code utilizes a similar outer layer finite state machine (Figure 6.2). In OFF state, variables and references are initialized, and a push button is polled at a low frequency looking for the

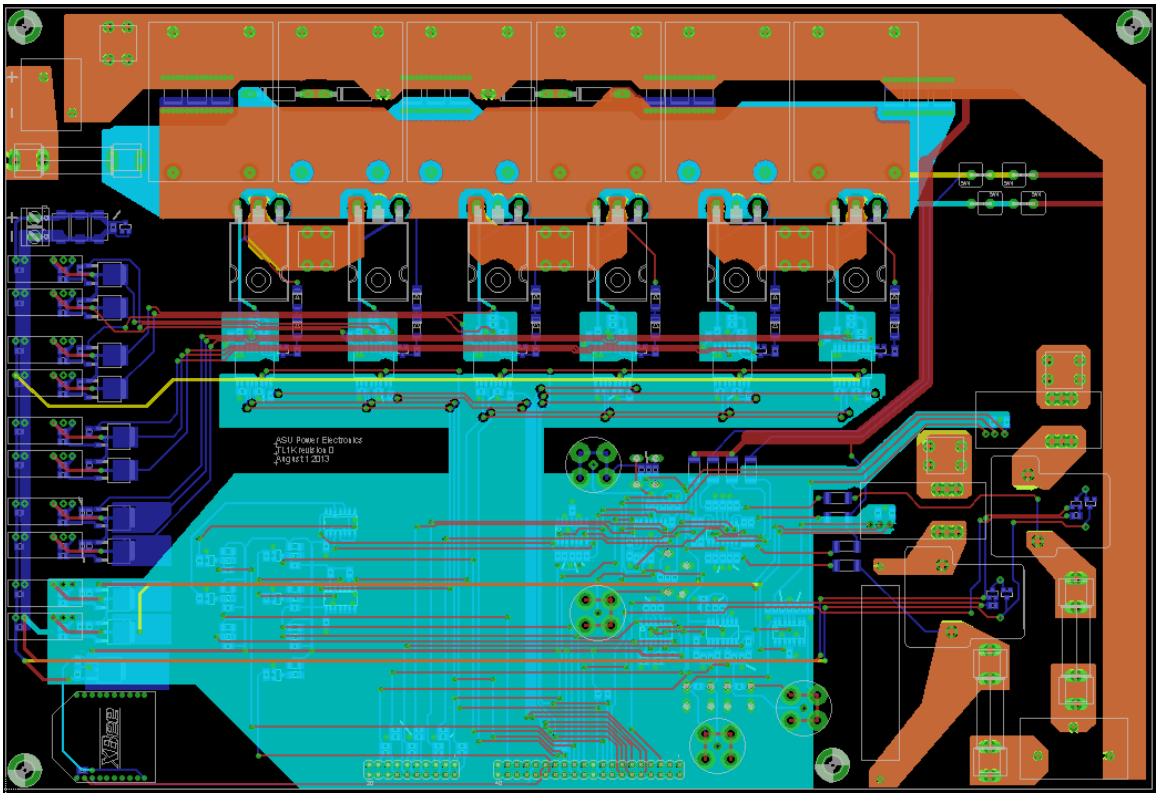

Figure 6.1: Power Circuit Printed Circuit Board

Table 6.2: Firmware Program Selection

| | |
|---|---|
| BB_OPEN | Buck boost converter open loop, inverters off |
| BB_CLOSED | Buck boost converter closed loop, inverters off |
| INV_OPEN1 | Inverters open loop at constant modulation index, buck boost at 50% duty |
| INV_OPEN2 | Inverters open loop, locked to grid (relays open), buck boost at 50% duty |
| INV_CLOSED | Inverters closed loop, buck boost converter at 50% duty |
| BOTH_CLOSED | Both loops closed |
| COMISSION | For checking out board and ADC calibration |
| DOUBLE_PULSE | For double pulse experiment |

start signal. Once a start has been initiated the system switches to INIT1 state. In this mode, appropriate converters are started and in some cases the PLL is locked to the grid for a short period of time. Upon leaving this mode, the controllers are started and the mode changes to INIT2 then to mode RUN. INIT2 is a second initialization step if needed. Within RUN mode, the control loops are closed and the push button is polled looking for turn off signal. Furthermore the low frequency timer also triggers data sent to the wireless communication module for display on a remote terminal.

The flow chart for normal closed loop operation is shown in Figures 6.3 and 6.4.

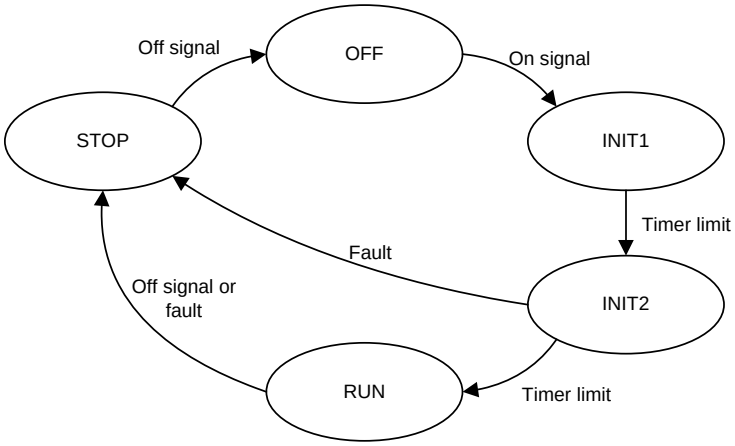


Figure 6.2: Outer Layer State Flow

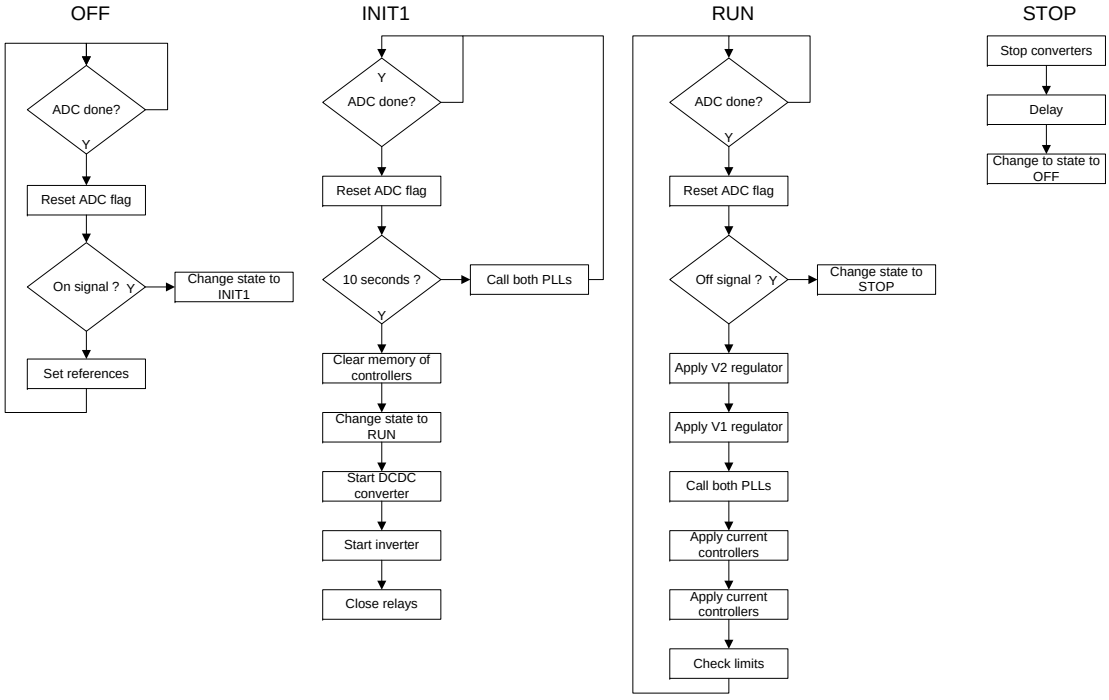


Figure 6.3: Flow Chart for Both Closed Mode

## 6.3 Experimental Results

An experiment was conducted in which the circuit was first connected to the grid with all control loops closed. A current source was applied at the input representing the PV array. The hardware configuration is illustrated in Figures 6.5, 6.6, and 6.7

After some troubleshooting, complete functionality was finally validated. The circuit maintained

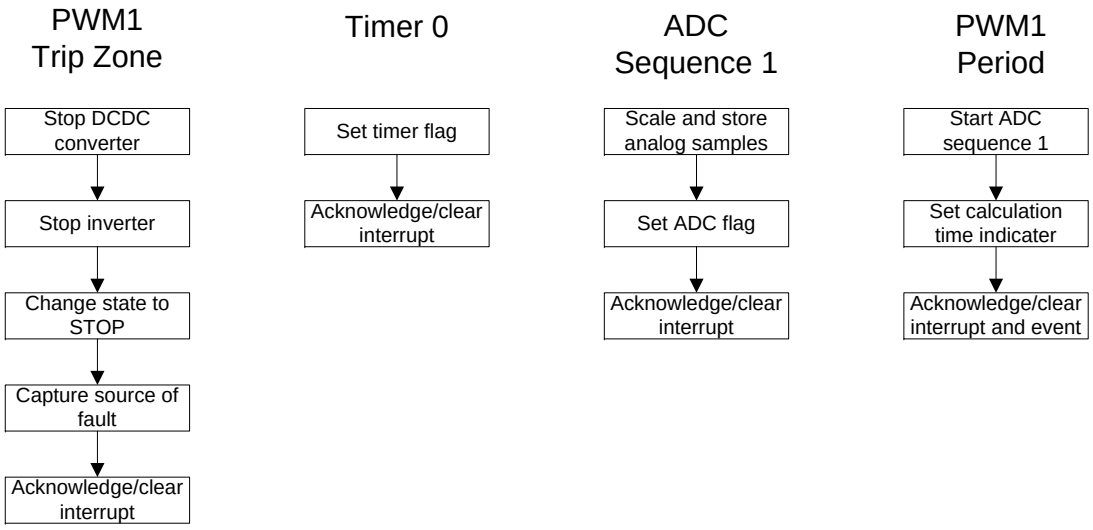


Figure 6.4: Flow Chart for Interrupts

power balance appropriately and fed current into the grid as expected.

Figure 6.8 shows the grid voltages and currents of each AC phase leg. The current includes some switching ripple because it is just an inductor filter. The corresponding simulations of Figure 6.9 shows sufficient match.

In Figure 6.10, the link voltages are illustrated in traces one and two corresponding to $v_1$ and $v_2$ respectively. The bottom side capacitor is buffering the double line frequency power as desired while the input voltage is tightly regulated. The corresponding simulation results are shown in Figure 6.11.

The buck boost inductor current of Figure 6.10 show some occasional spikes. These are the result of a periodic instability. Under certain conditions theses spikes were rather large and caused the inductors to emit significant audible noise. This instability is a result of the high bandwidth of the buck boost converter. As discussed in the chapter about the buck boost control system, the inductance varies with load conditions. The bandwidth and also phase margin are time varying. Under extreme conditions, the buck boost converter is unstable and the duty ratio saturates. This is an issue to be addressed. Some effort was made to correct the problem. Specifically a higher order controller with lower bandwidth was verified in simulation. However there was not enough processor time available to verify it in hardware.

Finally efficiency was measured at several input voltages. Results are shown in Figure 6.12.

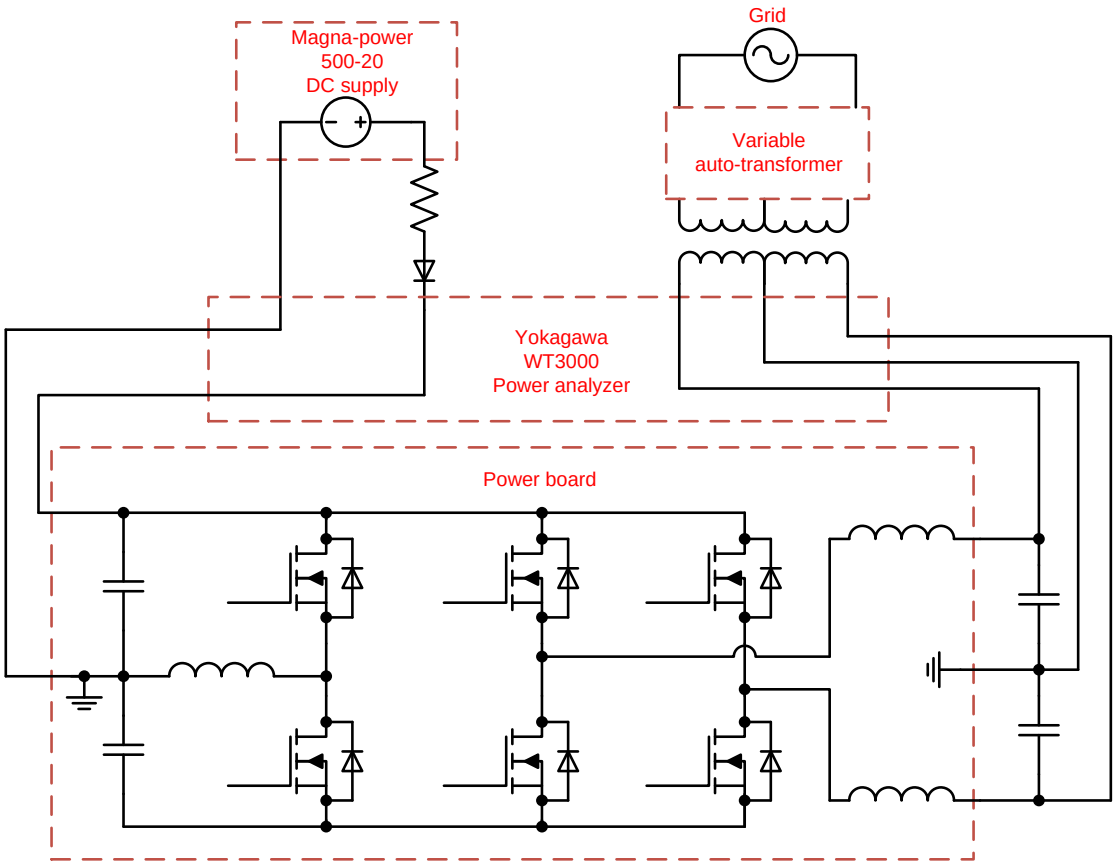


Figure 6.5: Basic Arrangement of Experiment Setup

Weighted California Energy Commission (CEC) efficiency [67] is given by equation (6.1). Table 6.3 gives the measured CEC efficiency at several input voltages with the bottom capacitor voltage regulated at $250\ V$. The measured efficiency is similar in shape, but better than predicted.

$$\eta = .04\eta_{10\%} + .05\eta_{20\%} + .12\eta_{30\%} + .21\eta_{50\%} + .53\eta_{75\%} + .05\eta_{100\%} \tag{6.1}$$

Table 6.3: Weighted CEC Efficiency at Several Input Voltages

| |
|---|
| $\eta_{200} = 97.3\%$ |
| $\eta_{300} = 96.9\%$ |
| $\eta_{400} = 96.4\%$ |
| $\eta_{475} = 95.9\%$ |

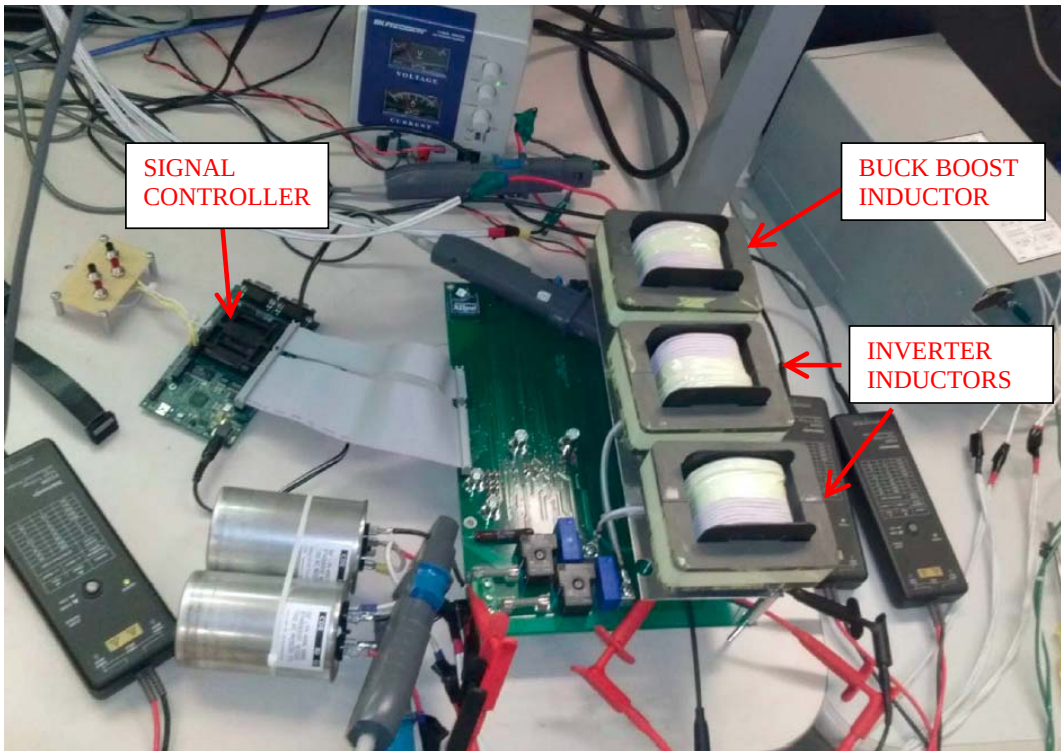


Figure 6.6: Experiment Hardware

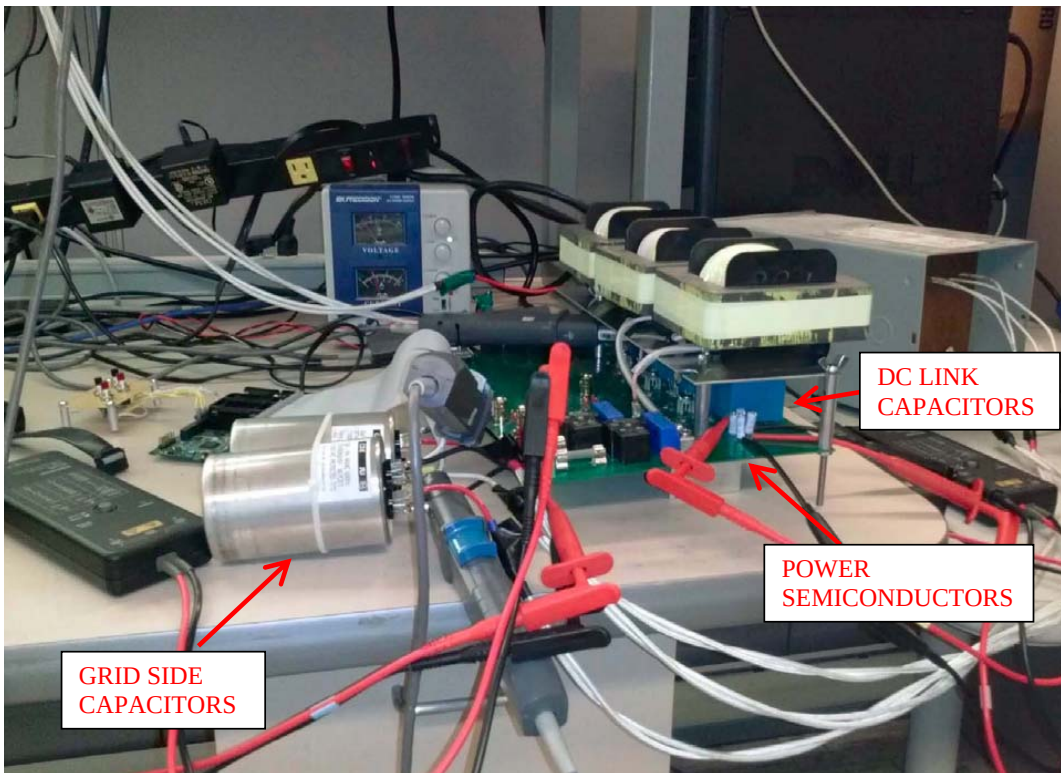


Figure 6.7: Experiment Hardware

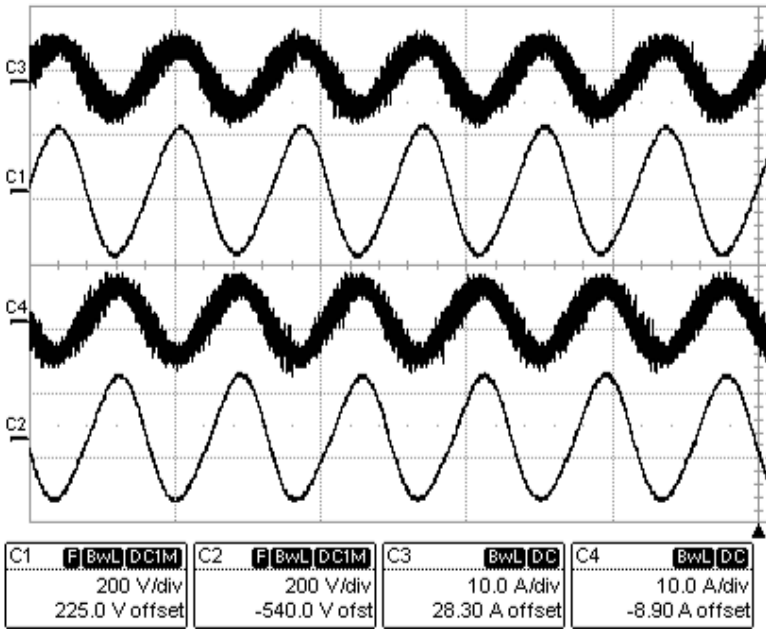


Figure 6.8: Experiment Waveforms: Line 1 Current, Line 1 Voltage, Line 2 Current, Line 2 Voltage

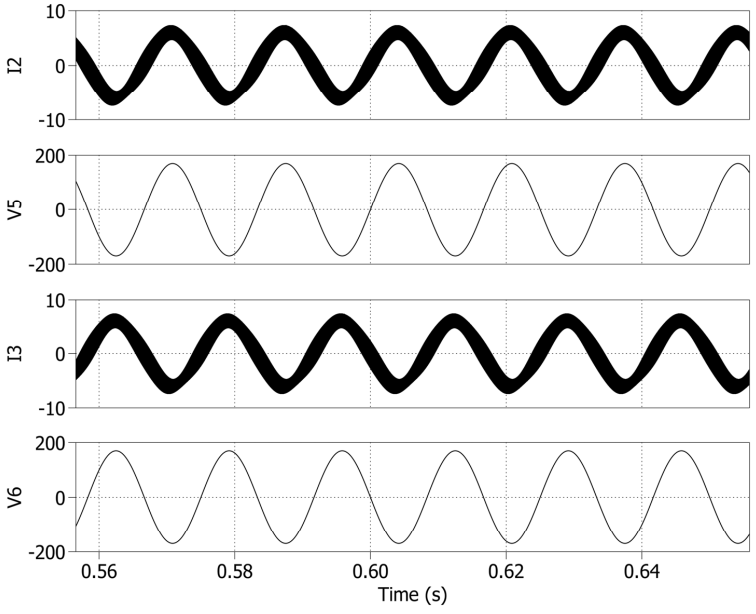


Figure 6.9: Simulation Waveforms: Line 1 Current, Line 1 Voltage, Line 2 Current, Line 2 Voltage

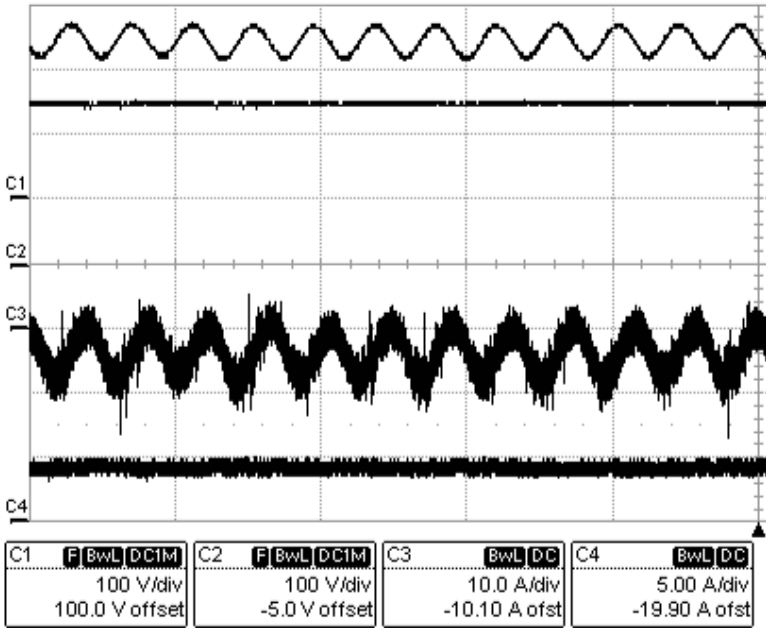


Figure 6.10: Measured Link and Input Waveforms: Input Voltage ($v_1$), Bottom Side Capacitor Voltage ($v_2$), Buck-Boost Inductor Current ($i_1$), Input Current ($i_4$)

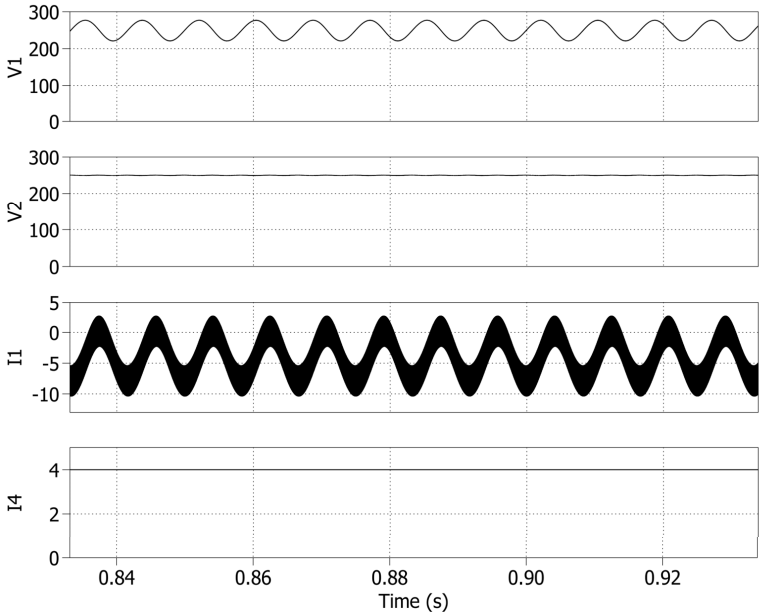


Figure 6.11: Simulations of Link and Input Waveforms: Input Voltage ($v_1$), Bottom Side Capacitor Voltage ($v_2$), Buck-Boost Inductor Current ($i_1$), Input Current ($i_4$)

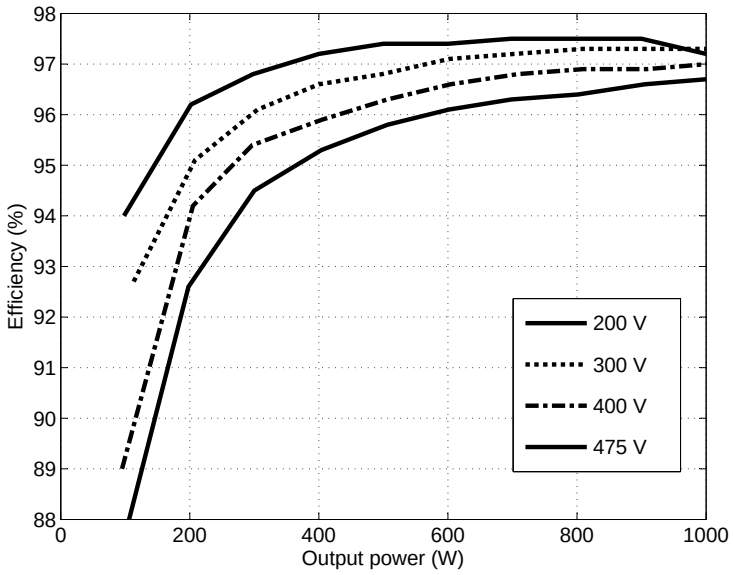


Figure 6.12: Efficiency Measurements at Several Input Voltages

# Chapter 7

# CONCLUSION

An original PV array inverter circuit and control system was discussed, simulated, and tested in hardware. Before introducing this new topology, the issues to be addressed were first presented. This included background discussion and literature review of single phase transformerless PV inverters and power decoupling of such inverters.

The proposed topology and control system were then presented as a solution. Other variants were also briefly mentioned. The power circuit of this study is comprised of a bi-directional buck boost converter and two half bridge inverters. The buck boost converter establishes a net DC link that is at most twice the input voltage. One of the capacitors of the buck boost converter absorbs double line frequency power pulsations; the other buck boost capacitor is at the input voltage potential and regulated constant. The half bridge inverters are fed by the net DC link from the buck boost converter. The two half bridge inverters create an alternating current to feed power into a balanced or unbalanced split phase residential type electric system.

The proposed circuit has numerous efficiency, reliability, and cost benefits compared with existing state of the art. Most importantly, elimination of the transformer results in a simpler circuit that is more efficient and less expensive than traditional inverters with line frequency transformers. The circuit exhibits zero leakage ground currents as a result the PV terminal's constant common mode potential relative to earth. Thus a large and expensive common mode filter is not needed. Also elaborate and risky switching sequences are not necessary. Reliability enhancement is made possible through the use of small film type capacitors and passive power decoupling on the DC link. Furthermore the circuit has fewer semiconductors than comparable transformerless inverters. This topology is realizable in an efficient way with silicon carbide transistors.

The energy storage elements were first carefully selected for the particular application. The primary objective was to design the circuit with low capacitance on the DC rails to permit the use of more reliable film type capacitors. The inductors were designed for low core and copper losses.

A unique control system was then developed to attain the desired operational and performance characteristics. The input voltage regulator was arranged to track DC references from the Maximum Power Point Tracking (MPPT) algorithm. The input voltage regulator also attenuates double line frequency currents with a resonant term. The bottom side capacitor voltage regulator was configured with

a low bandwidth to track only the DC reference and permit double line frequency voltage ripple for power decoupling purposes. The grid current control system was configured as a proportional resonant type to track line frequency current references. The control system along with the power circuit configuration are the original contributions of this research.

An analytic efficiency analysis was conducted to approximate how the circuit might perform. This includes losses from semiconductor and magnetic components. Both switching and conduction losses of the silicon carbide transistors were considered. Core losses of the inductors were approximated with an empirical formula provided by the manufacturer. The net efficiency was predicted at several operating conditions. Also losses associated with each individual component were presented graphically. The efficiency model still needs refinement because it was found to be rather complicated and not very accurate.

Many simulations were conducted to verify and adjust the design as needed. A design script was developed concurrently with the simulation development to model the control system, hardware circuit, and create firmware constants. The buck boost converter and inverters were first simulated separately while subject to various disturbance and operating conditions. The circuits were then combined as they would be in the actual prototype. The complete circuit was then simulated and verified under various voltage and power conditions that might occur in a real application.

An prototype was then constructed to prove the concept. A custom circuit board was drafted to hold the power semiconductors, power capacitors, signal conditioning, and fault detection circuitry. The program firmware was implemented on a separate signal controller board. The boards were wired together along with the magnetic components and after some adjustments complete functionality was verified up to about $1200\ W$. Experiment results were close to predicted. The peak measured CEC weighted efficiency was over $97\%$. Also an optimal switching frequency was approximated from a series of experiments.

The primary disadvantage of the topology is that half the DC link voltage follows the maximum power point of the array. This can lead to large voltage stress and increased inductor/transistor losses under certain conditions. Also with the bottom side capacitor exhibiting double line frequency voltage swings when heavily loaded, it is difficult but not impossible to avoid resultant grid current distortions.

There are a few aspects of the circuit that still need improvement. The average voltage across the bottom side capacitor may be scheduled for optimal performance and further reduction of the re-

quired bottom side capacitance. A higher order (LCL) grid side filter would result in reduced inductance requirements for a given harmonic content. Efficiency could be investigated further analytically, with simulation tools, and in experiment to optimize design trade-offs. A design optimization as in [1] would be a useful refinement. Anti-islanding features [68] would be necessary for a final product. Furthermore a efficiency comparison with existing state of the art converters would provide useful information about the circuit's viability in the market place. Results indicate this is however a viable and competitive power converter circuit for string type PV arrays.

Chapter 8

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